

COMPAL CONFIDENTIAL

MODEL NAME : CDP70
PCB NO : LA-E141P
BOM P/N :
GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge 14 UMA

Kabylake H


2016-07-01

REV : 0.2 (X01)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESD Component
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- XDP@ : XDP Component
- CONN@ : Connector Component

MB PCB	
Part Number	Description
DAB0001R000	PCB 1SC LA-E141P REV0 MB UMA 1

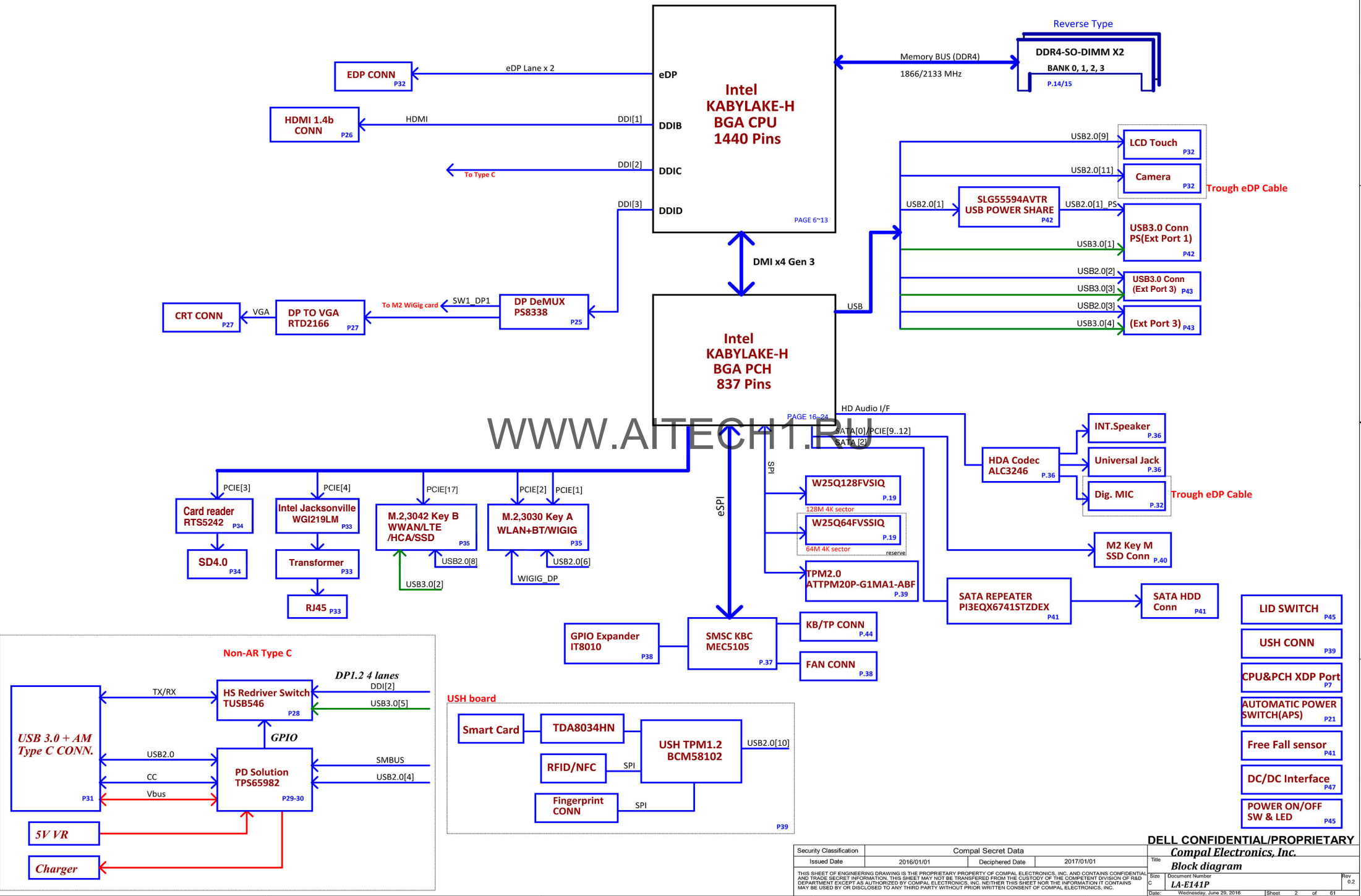
Layout Dell logo

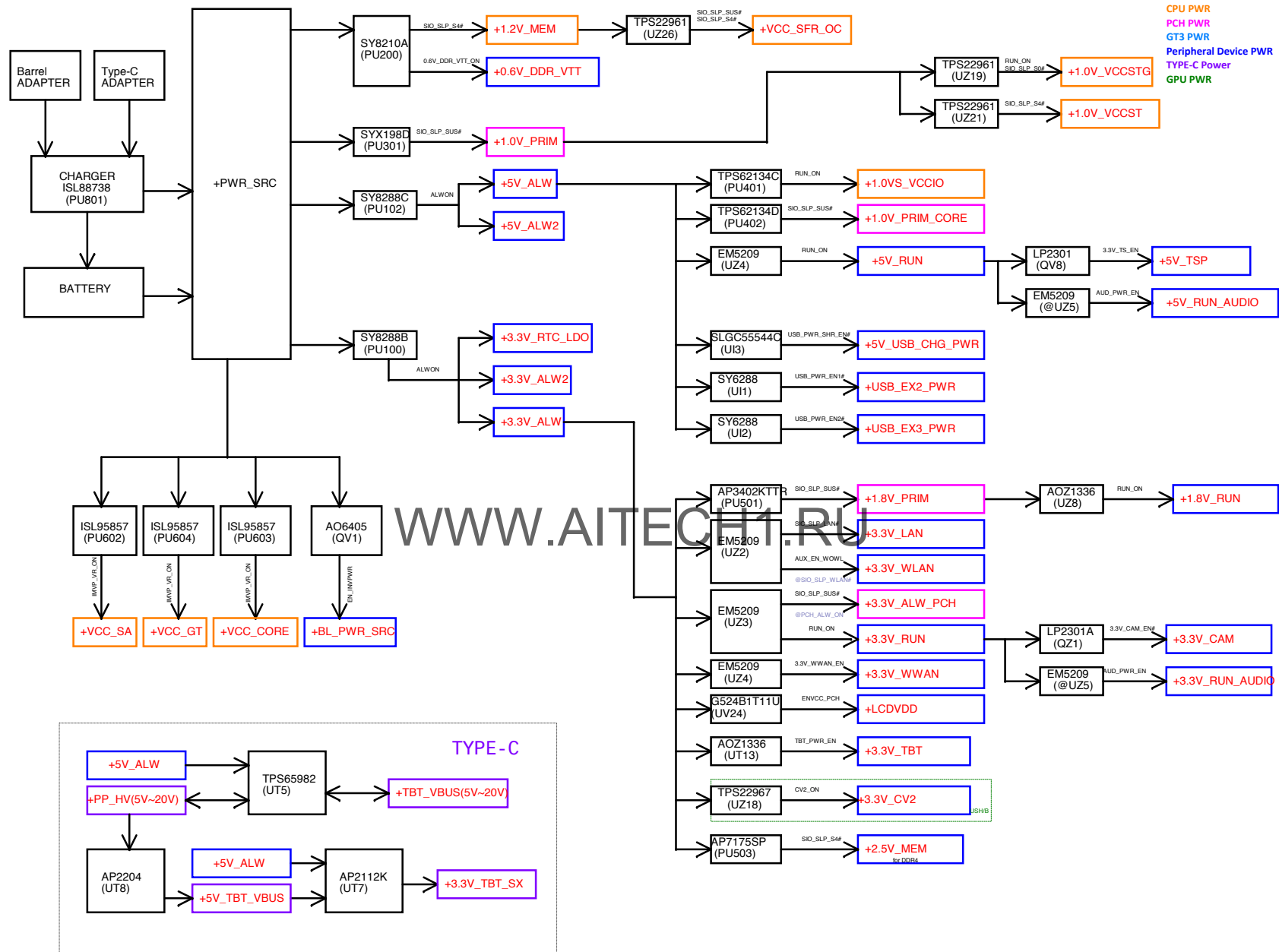


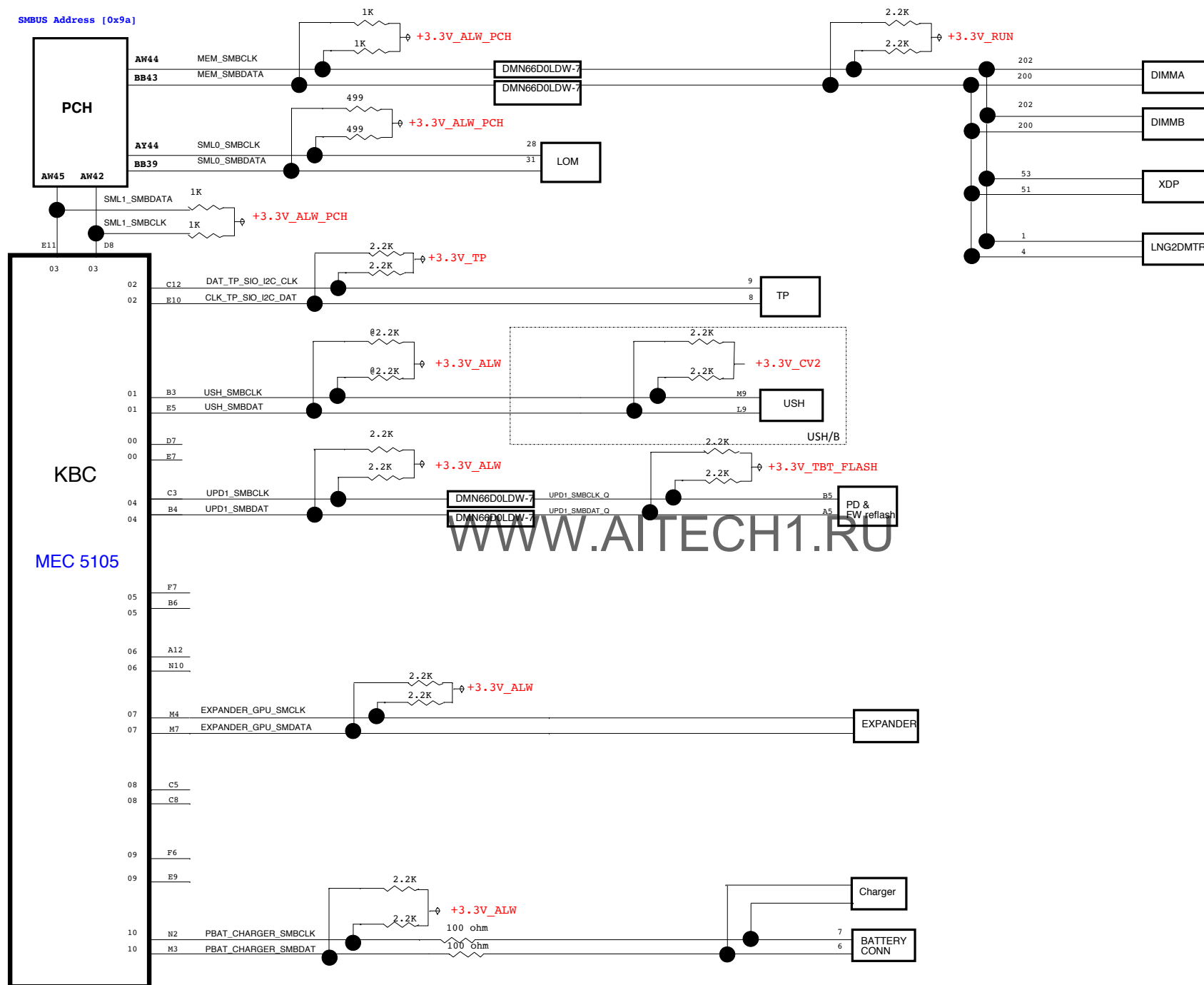
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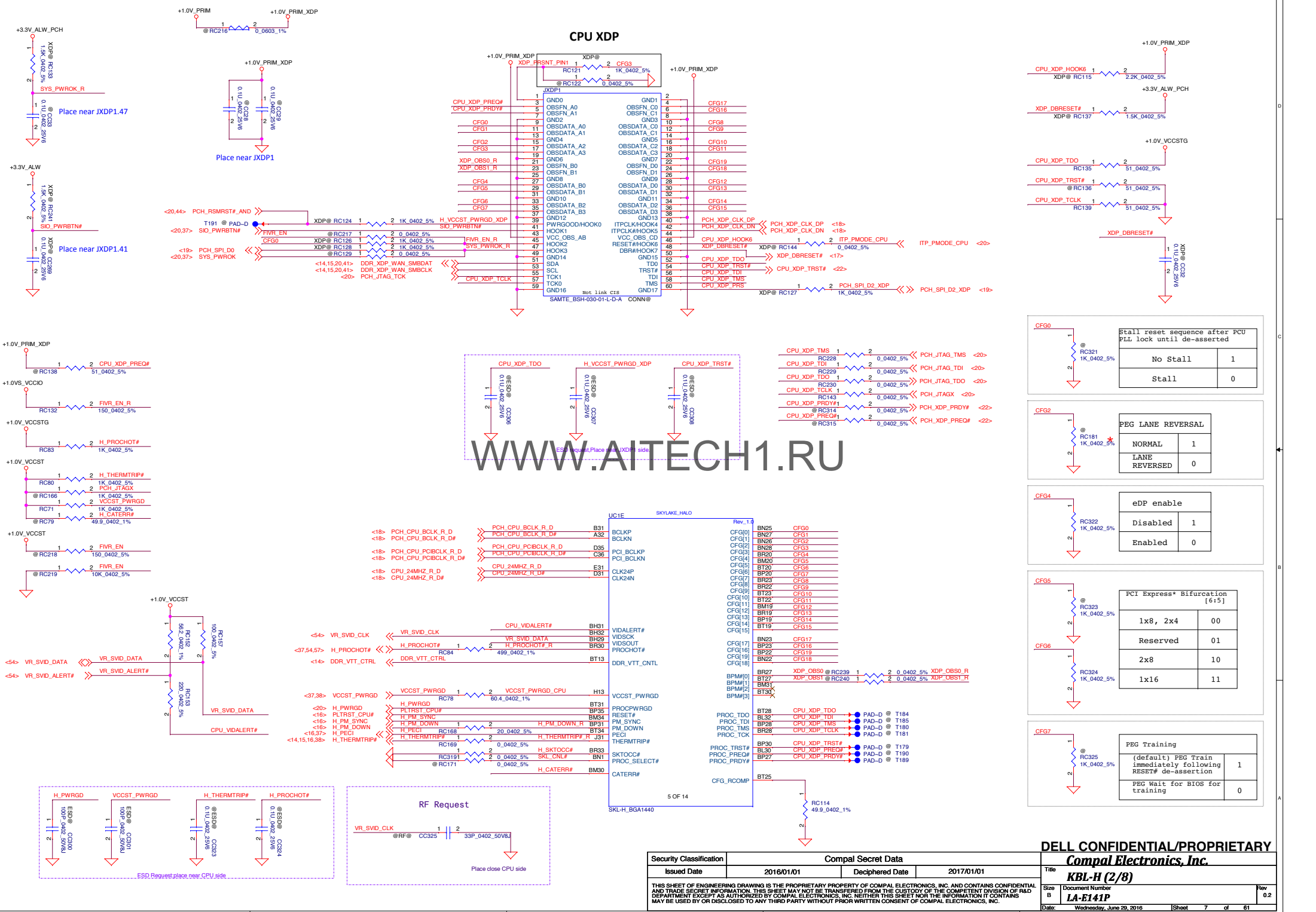
Breckenridge 14 UMA non-TBT Block Diagram







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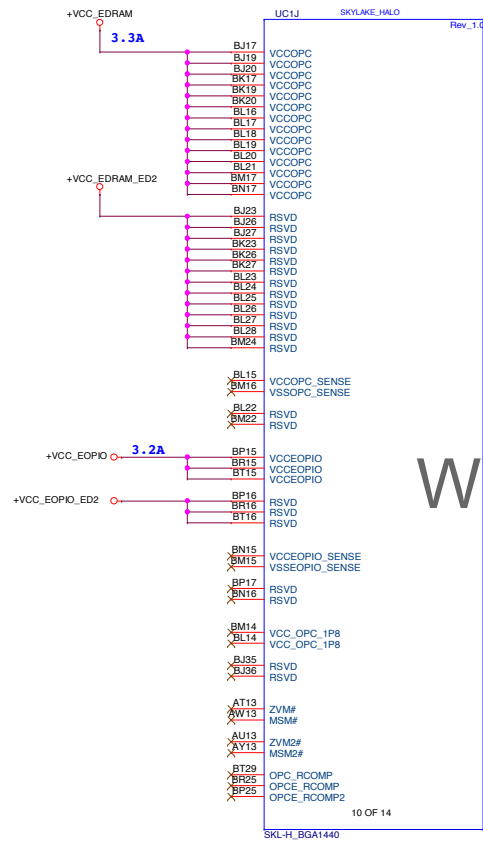


CPU XDP

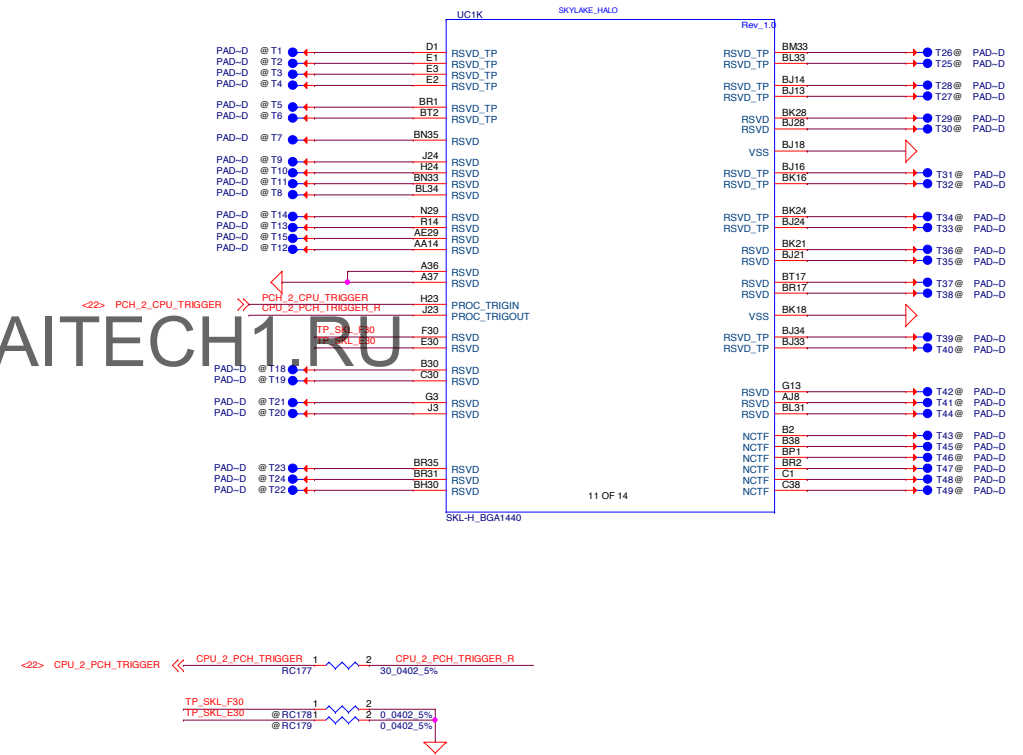
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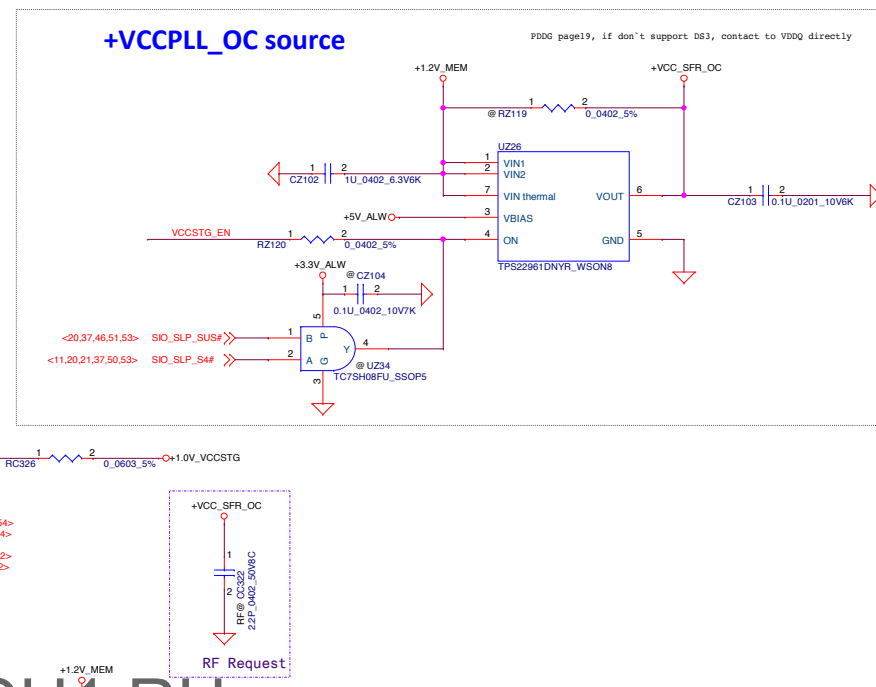
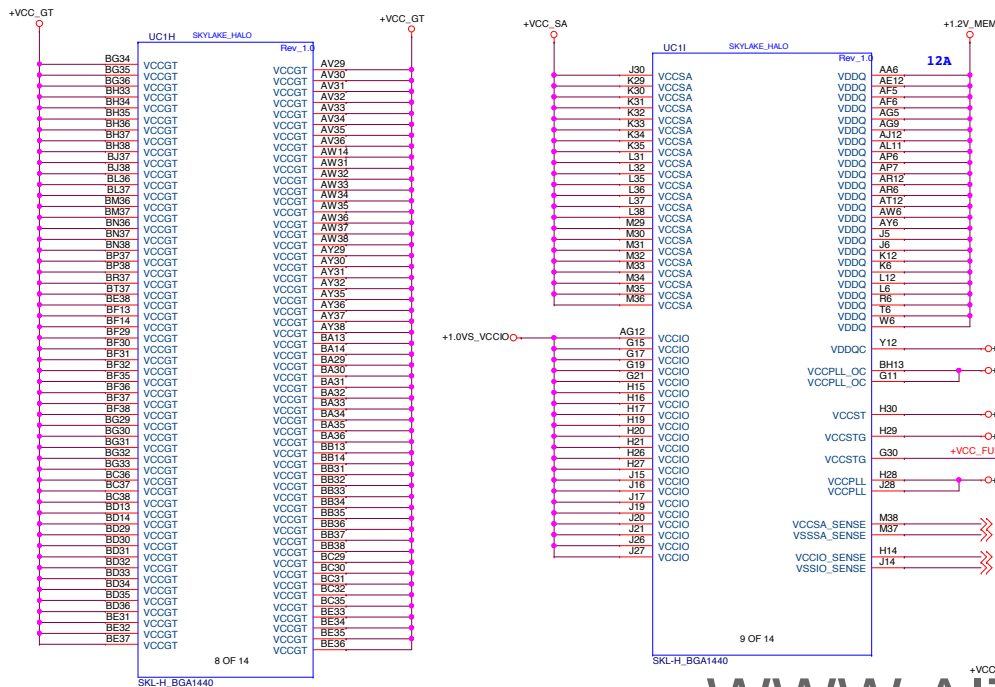


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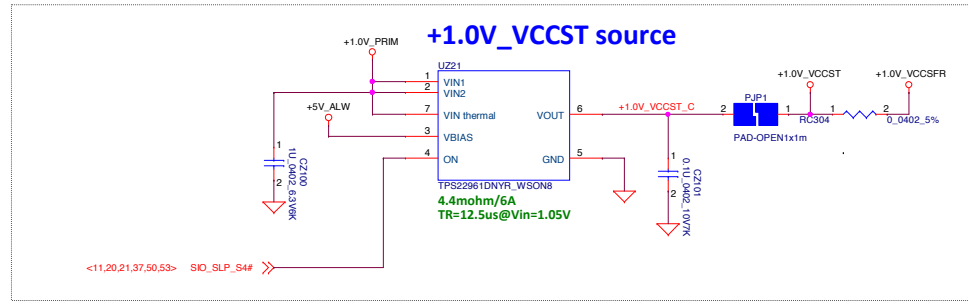
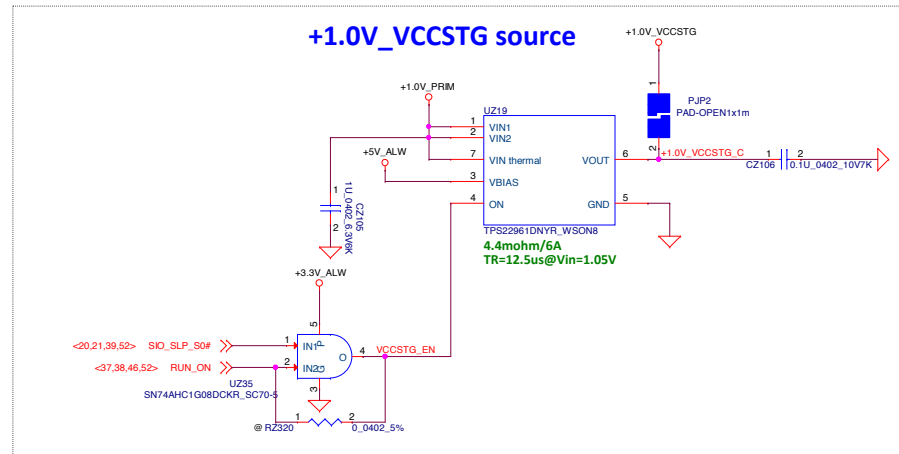


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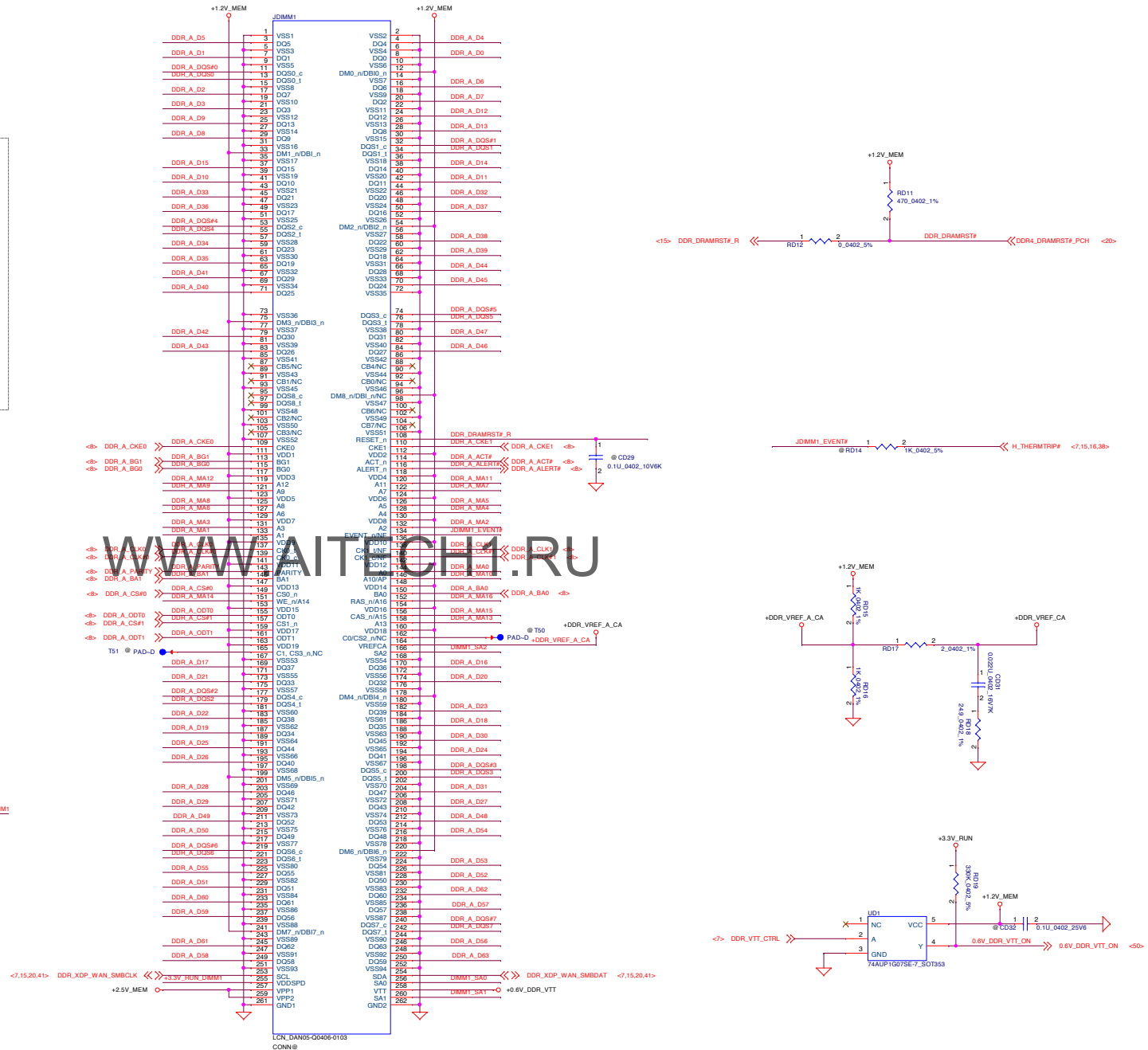
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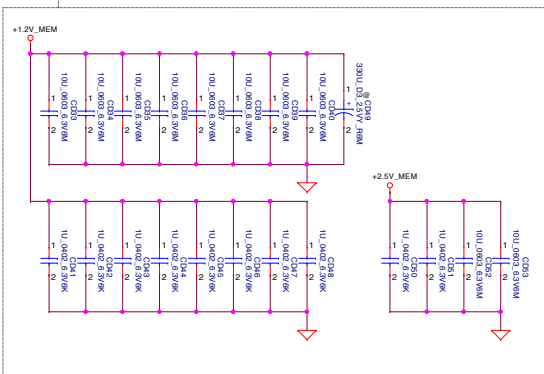


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Byte[1]	DQ[15:8]	DQS/DQS# [1]
Byte[2]	DQ[23:16]	DQS/DQS# [2]
Byte[3]	DQ[31:24]	DQS/DQS# [3]
Byte[4]	DQ[39:32]	DQS/DQS# [4]
Byte[5]	DQ[47:40]	DQS/DQS# [5]
Byte[6]	DQ[55:48]	DQS/DQS# [6]
Byte[7]	DQ[63:56]	DQS/DQS# [7]

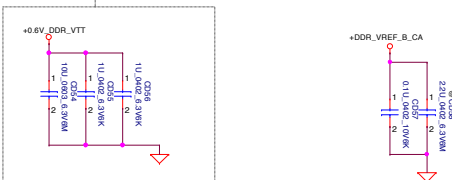


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 <> DDR_B_DQS#0..7
 <> DDR_B_DQ15..31
 <> DDR_B_DQ15..31
 <> DDR_B_DQ32..47
 <> DDR_B_DQ32..47
 <> DDR_B_DQ48..63
 <> DDR_B_DQ48..63

Layout Note:
Place near J1DIMM2

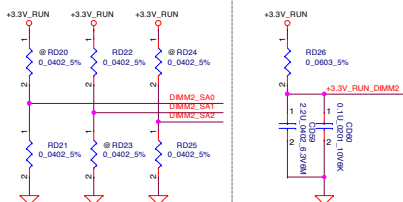


Layout Note:
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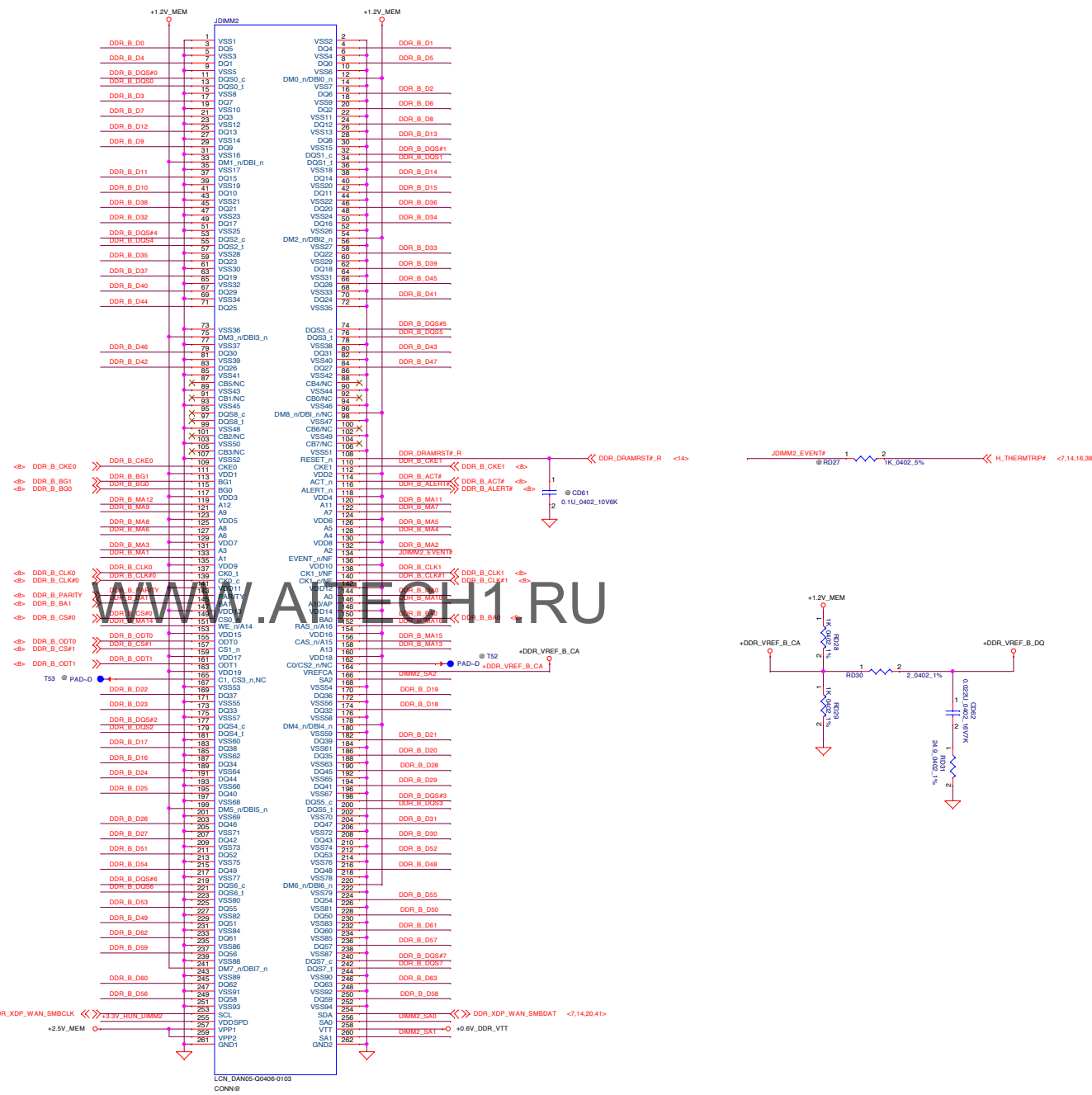


DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
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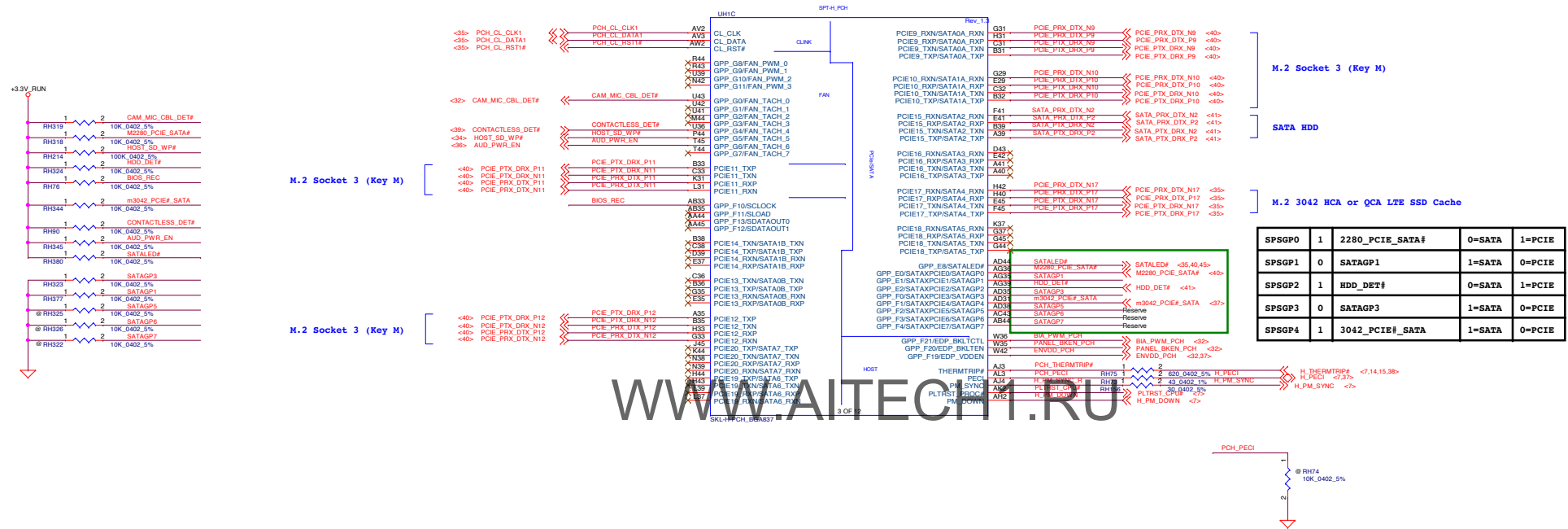


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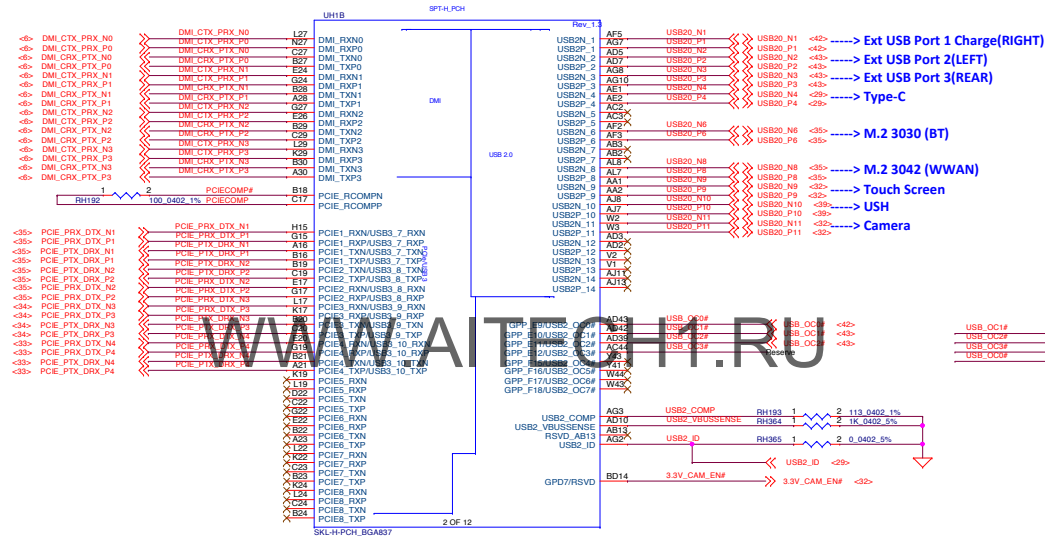
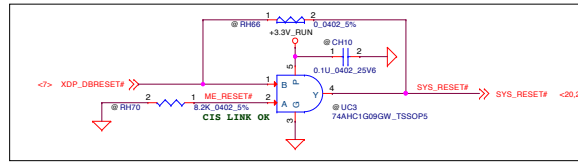
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DDR4-SODIMM SLOT2

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SPSGP0	1	2280_PCIE_SATA#	0=SATA	1=PCIE
SPSGP1	0	SATAGP1	1=SATA	0=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	1=SATA	0=PCIE
SPSGP4	1	3042_PCIE#_SATA	1=SATA	0=PCIE

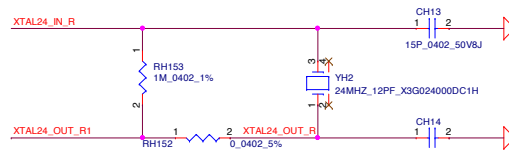
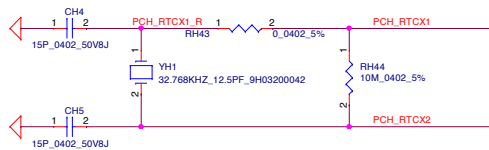
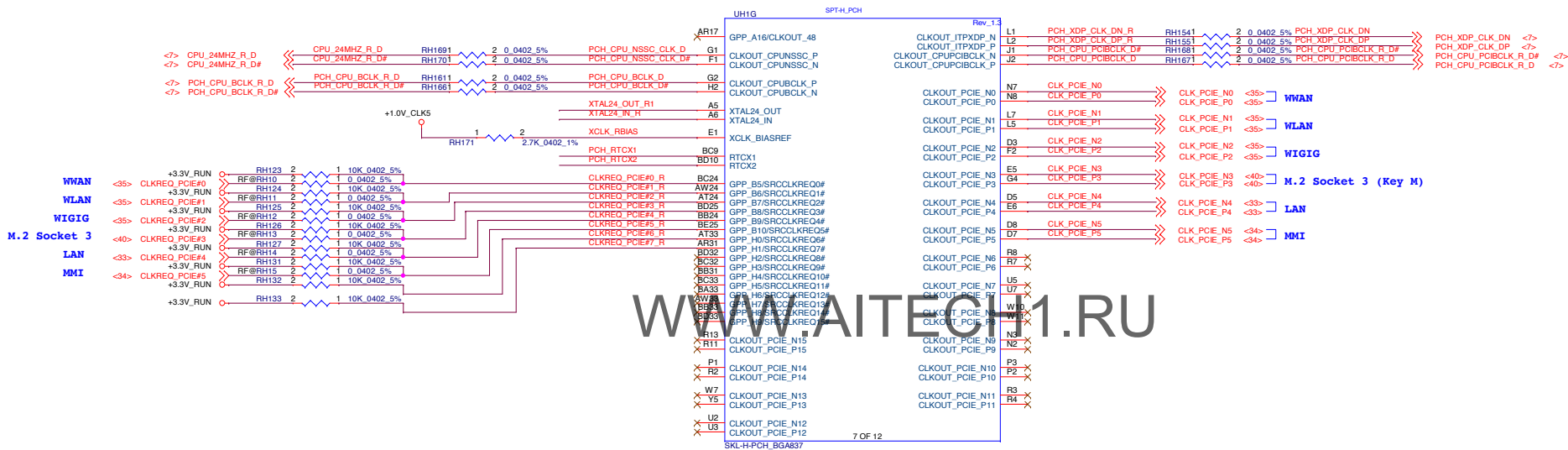


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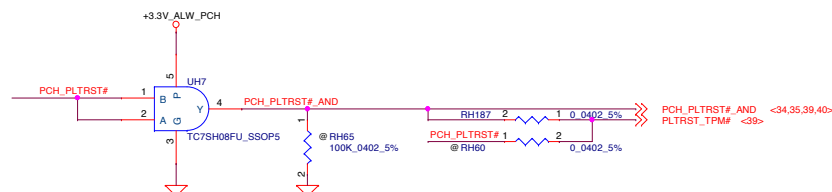
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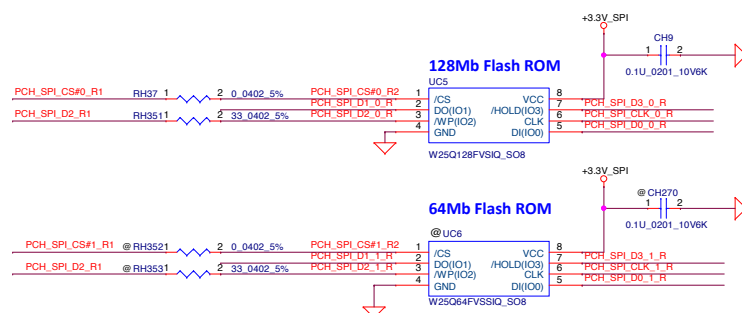
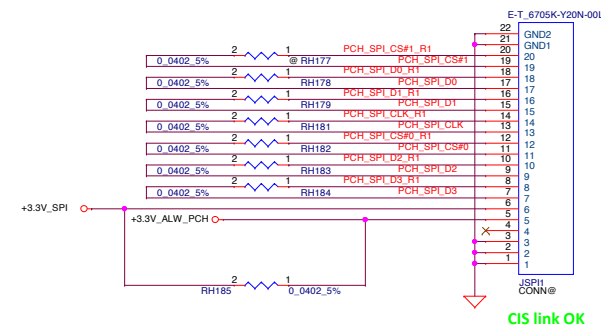
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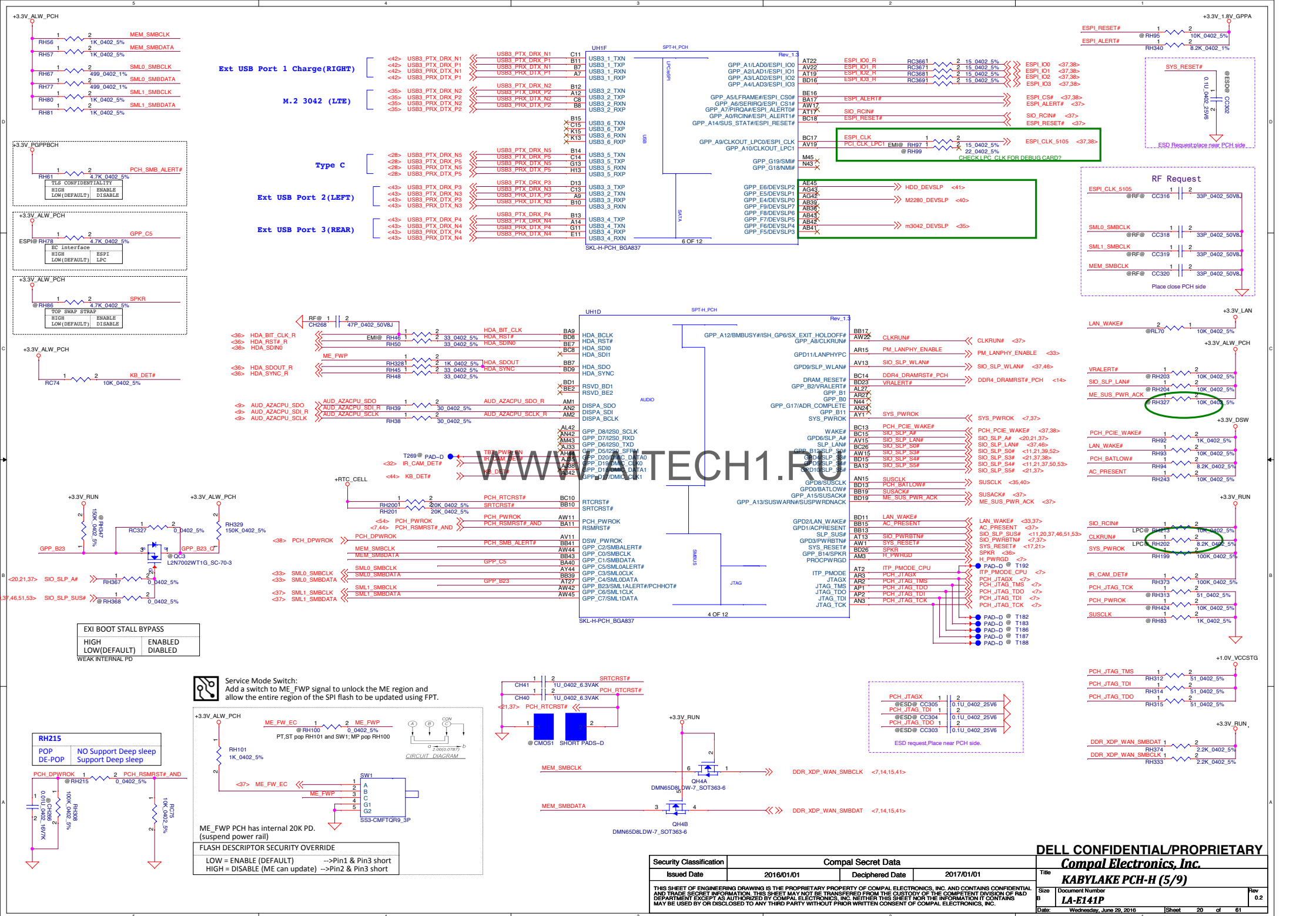
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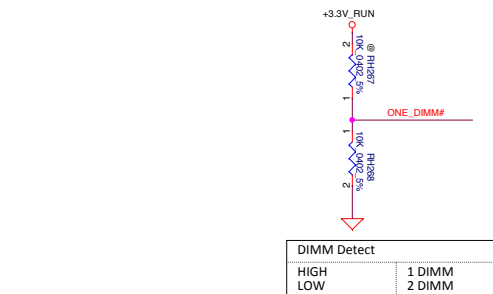
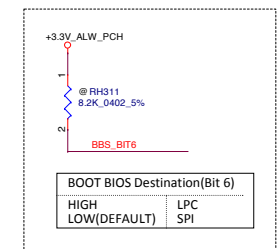
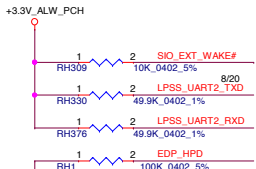
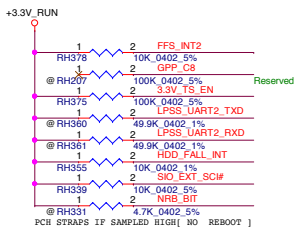


Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

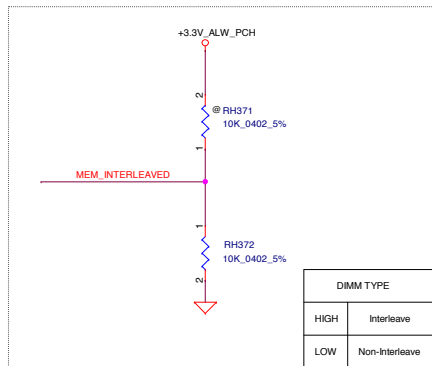
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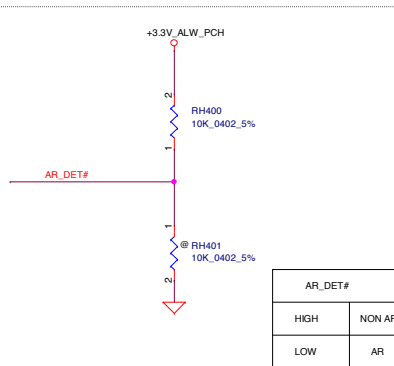




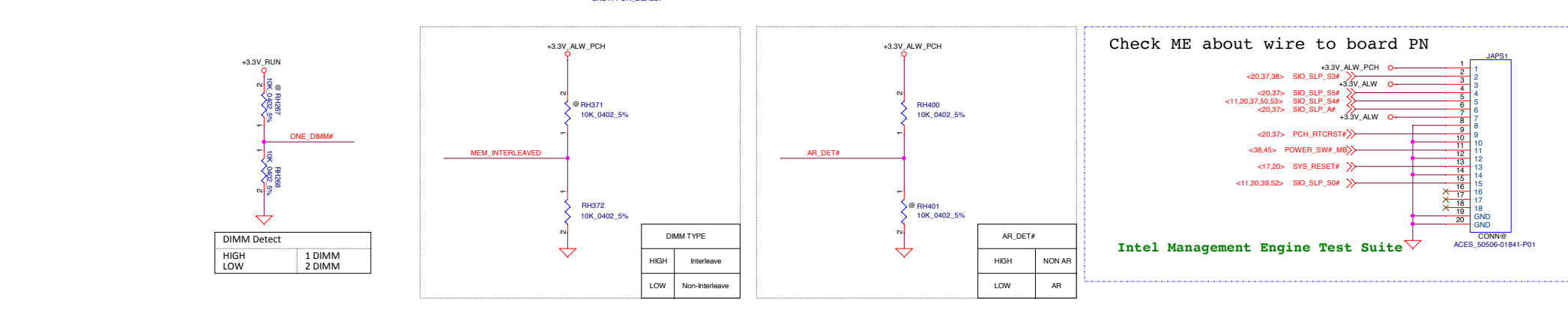
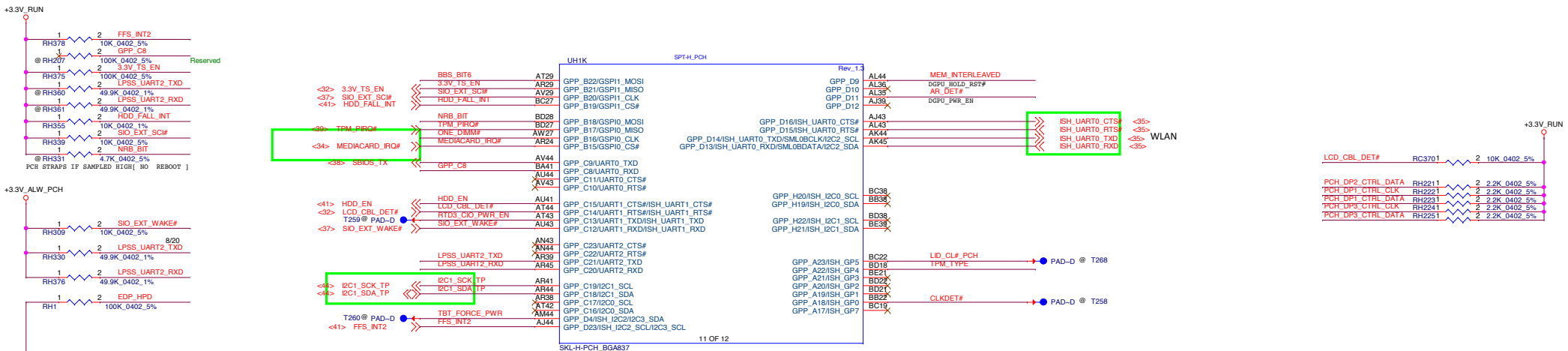
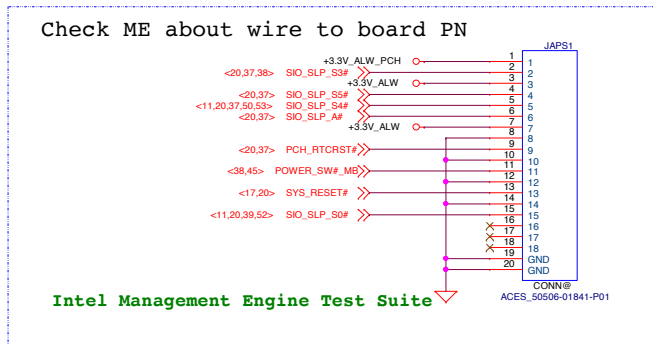
DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

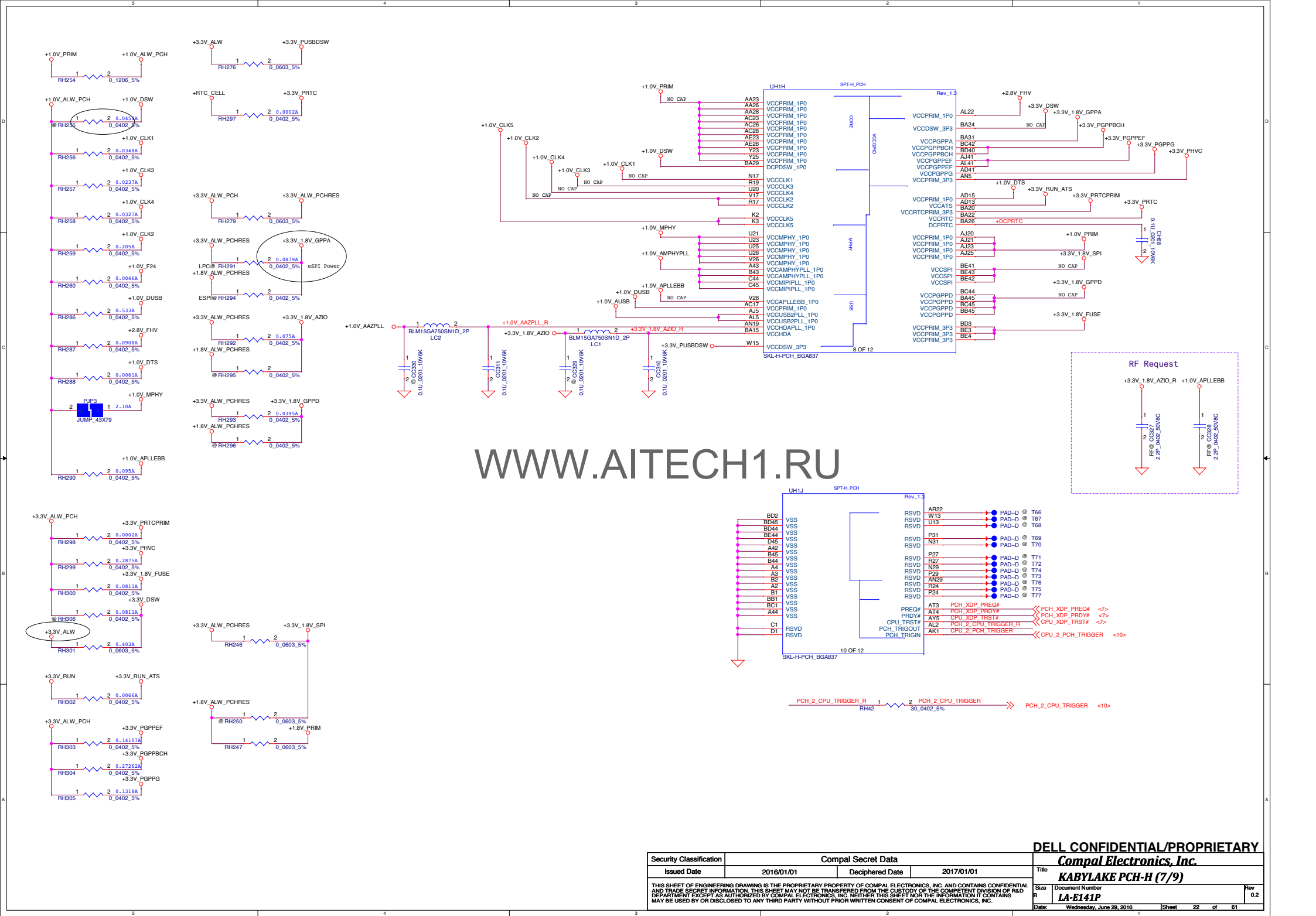


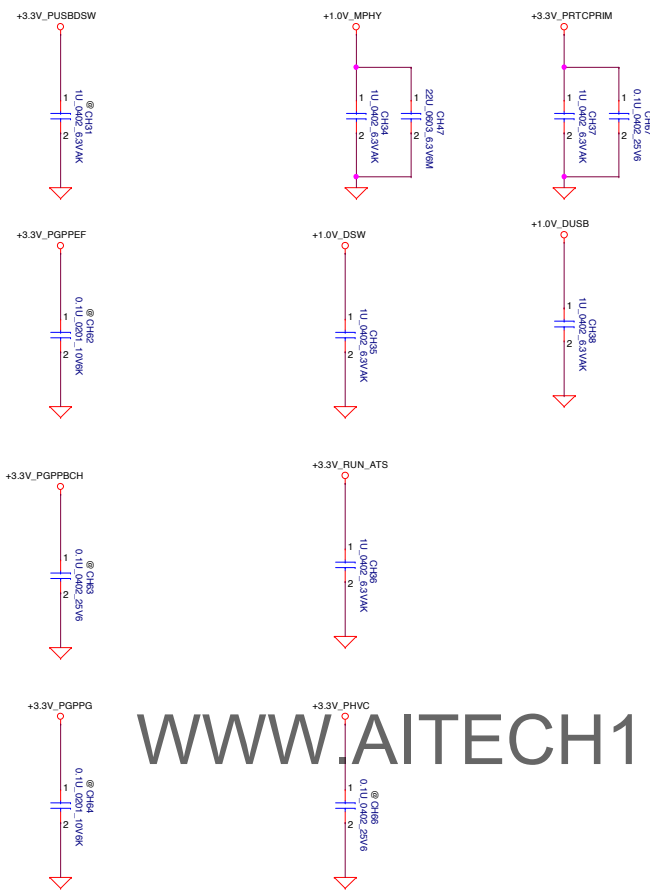
DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave



AR_DET#	
HIGH	NON AR
LOW	AR

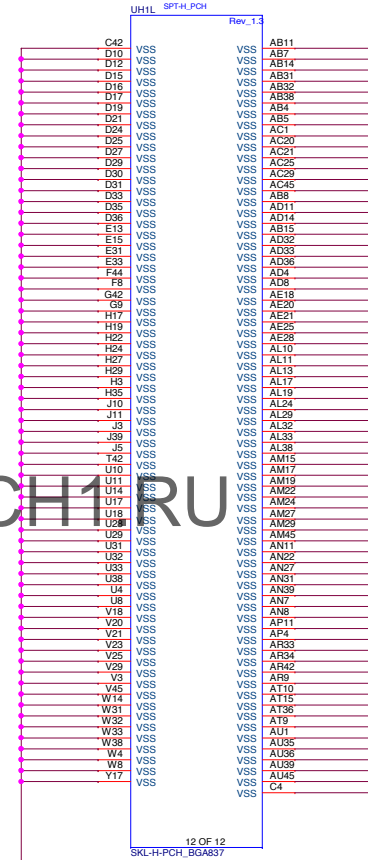
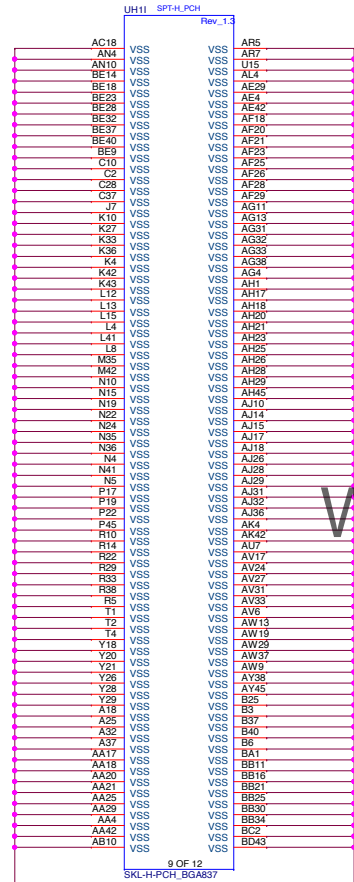






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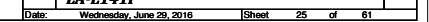
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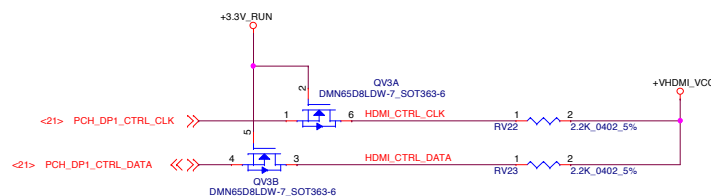
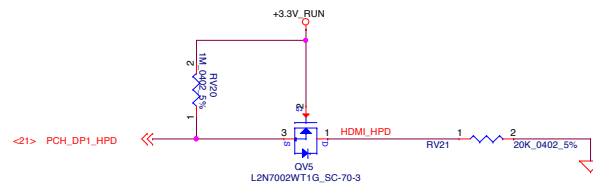
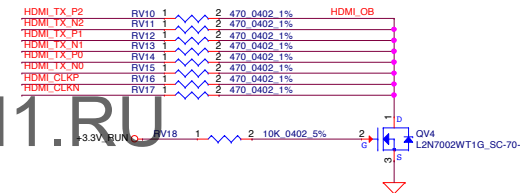
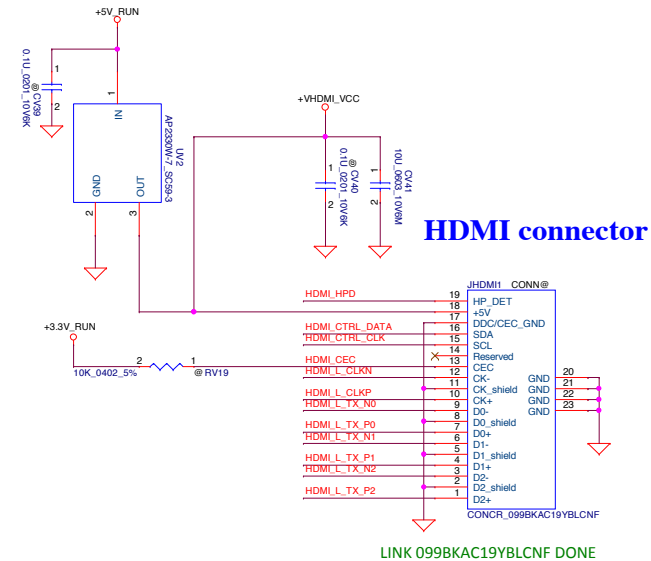
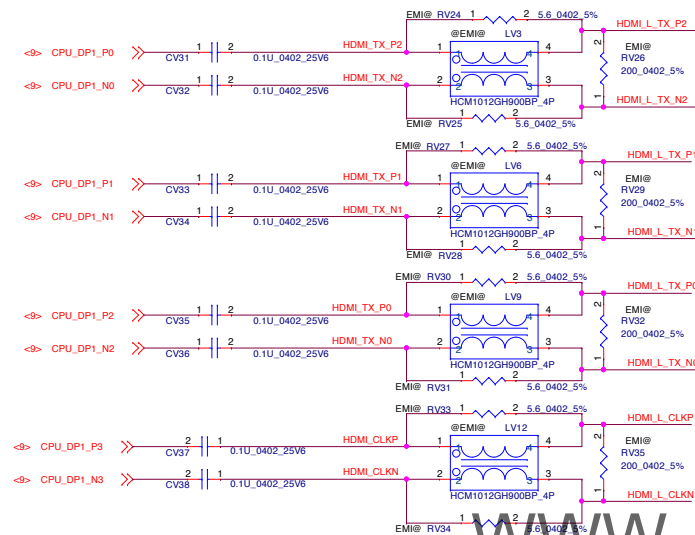
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For Breckenridge 14



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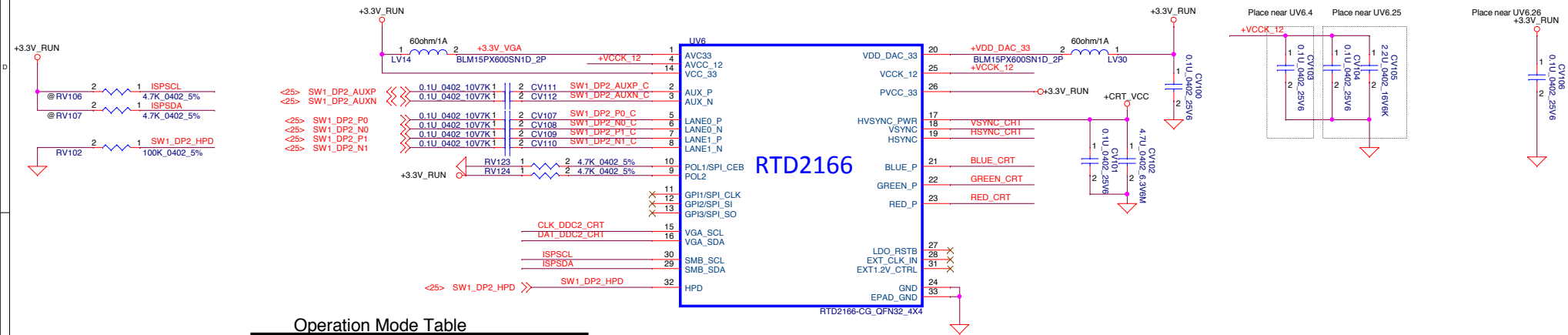
HDMI CONN

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For TBT SW2_DP2
For non-TBT SW1_DP2

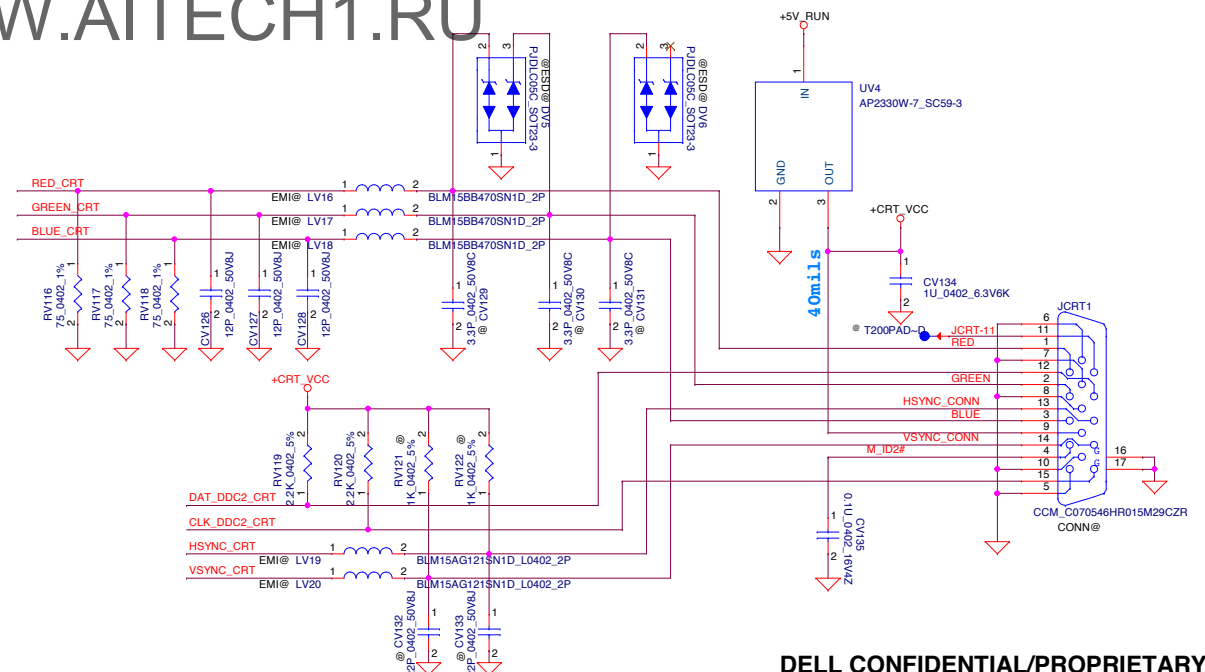
For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM

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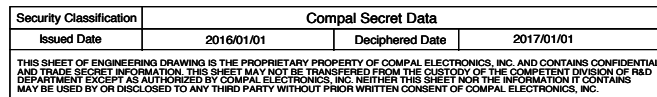
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DP to VGA & VGA Conn

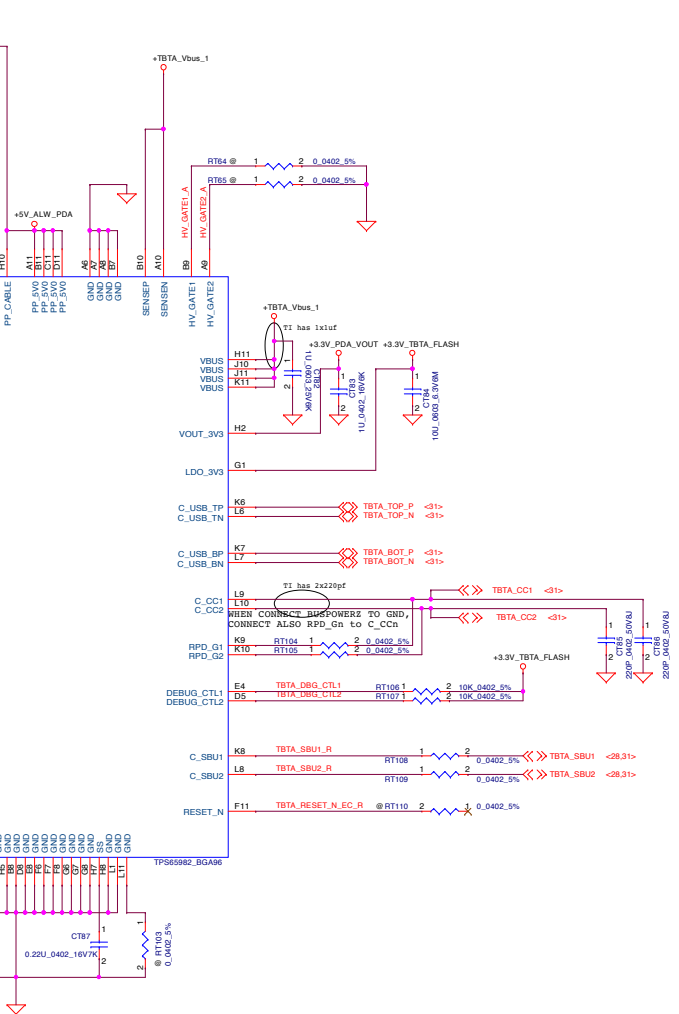
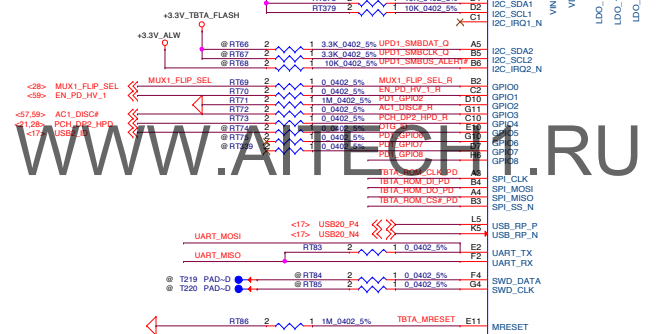
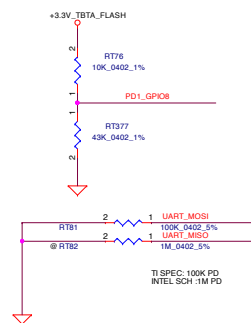
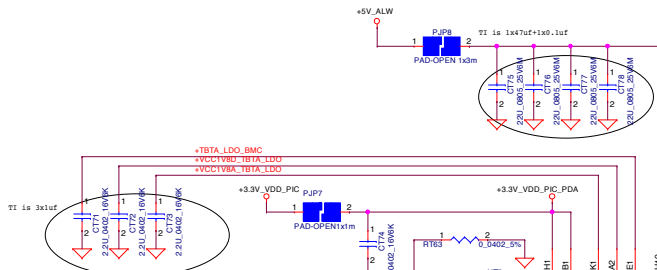
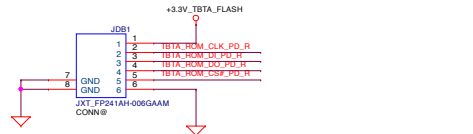
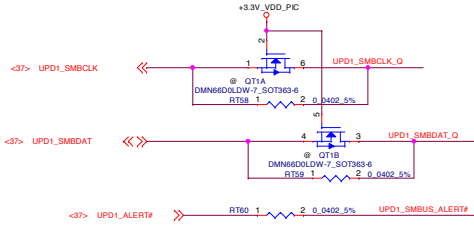
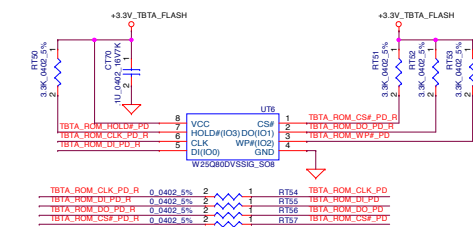
Document Number
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Rev
0.2

Date: Wednesday, June 29, 2016 Sheet 27 of 61

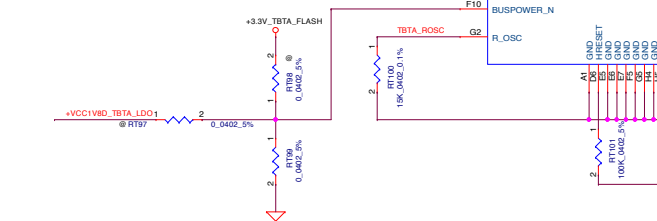
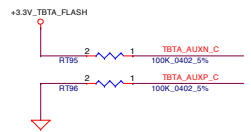


For Non-AR config



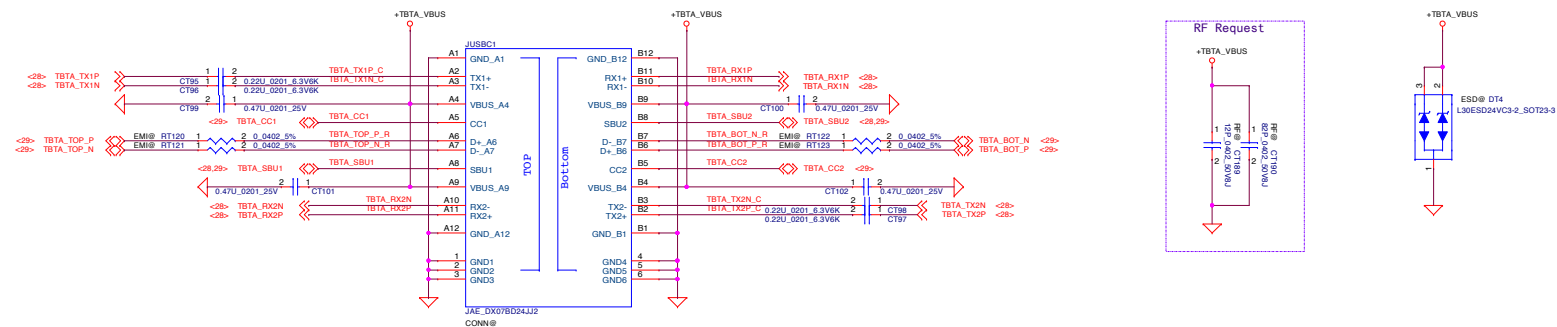
DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	<p>UEP only</p> <p>SV @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>Ti VID supported</p>
0.10	0.18	1	<p>UEP only</p> <p>SV @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes -Sink, C and D pin configuration Ti VID supported</p>
0.20	0.28	2	<p>UEP only</p> <p>SV @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>Ti VID supported</p>
0.30	0.38	3	<p>UEP only</p> <p>SV @0.9A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes -Sink, C and D pin configuration Ti VID supported</p>
0.40	0.48	4	<p>DPP</p> <p>SV @0.9-3.0A Sink capability</p> <p>SV @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>Ti VID supported</p> <p>Accepts data and power role swaps, but does not initiate.</p>
0.50	0.58	5	<p>DPP</p> <p>SV @0.9-3.0A Sink capability</p> <p>SV @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes - Source, C, D, and E pin configurations.</p> <p>Ti VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p><u>Accepts data role swap to UEP- and can initiate.</u></p>
0.60	0.68	6	<p>DPP</p> <p>SV @0.9-3.0A Sink capability</p> <p>SV @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes - Source, C, D, and E pin configurations.</p> <p>Ti VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p><u>Accepts data role swap to UEP- and can initiate.</u></p>
0.70	1.00	7	Infinite boot retry from Flash to Host IF cycles.

Route in pass through manner so AUX can be snooped by 546

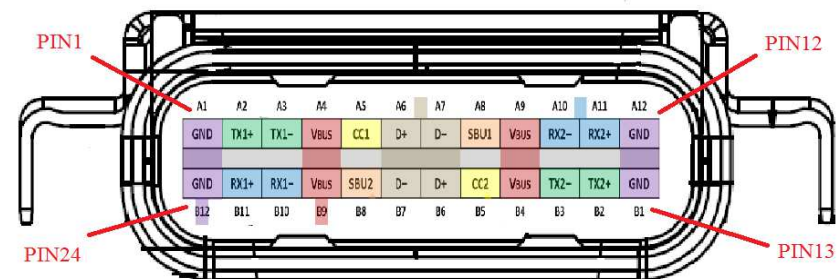
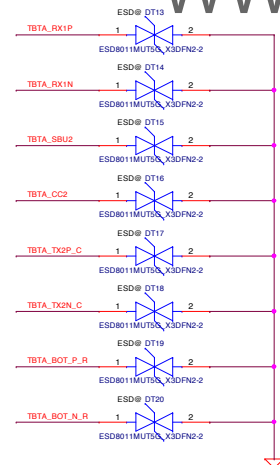
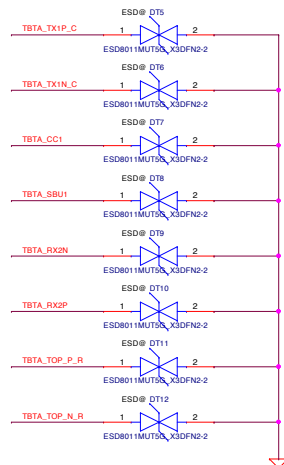


Need Link TPS65982D

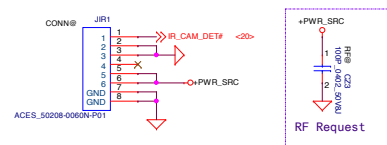
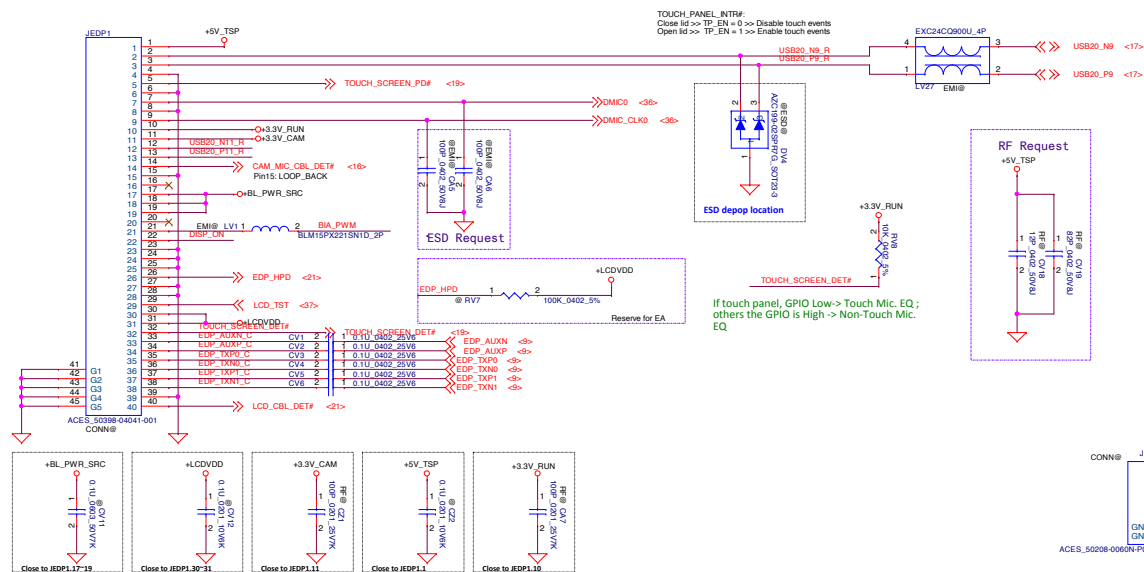
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Issued Date	2016/01/01	Deciphered Date	2017/01/01	Title	<div> <div>Compal Electronics, Inc.</div> <div>[Type] C/PD Controller TI</div> </div>
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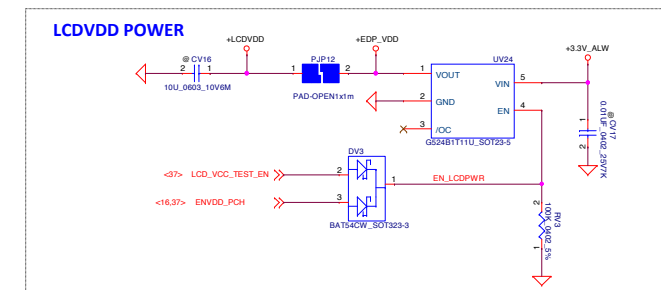
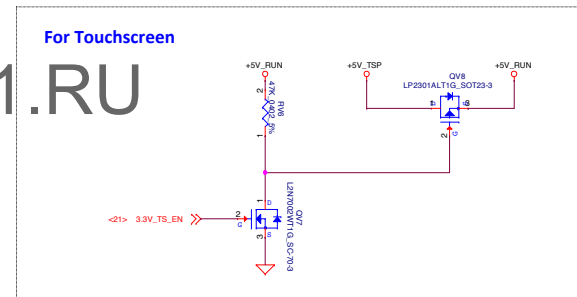
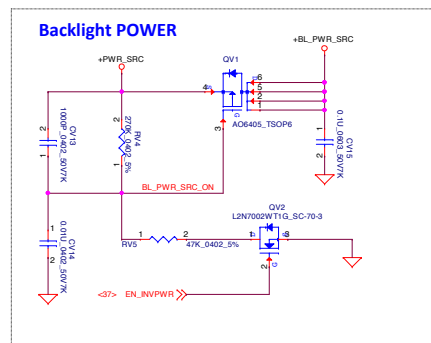
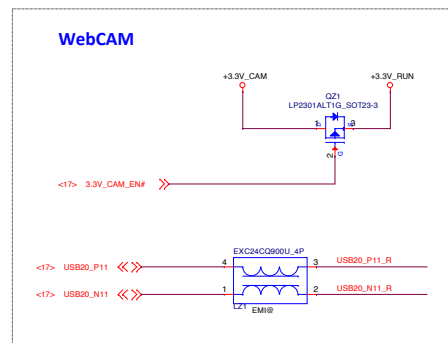
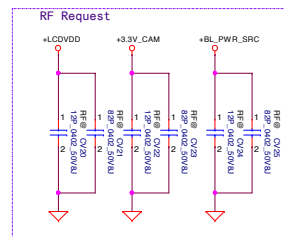
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For Breckenridge 14



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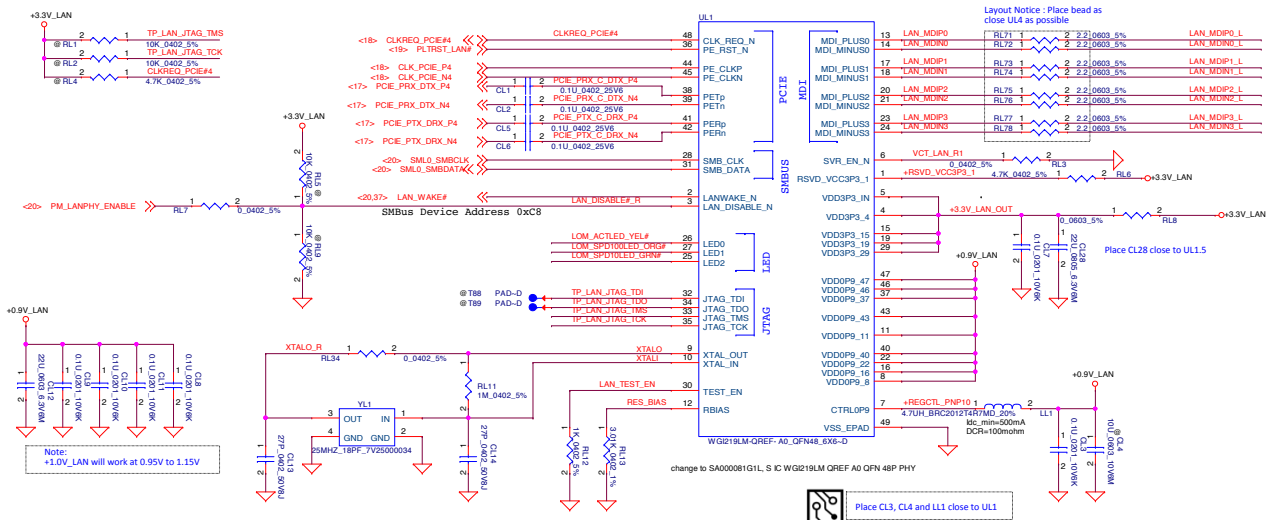


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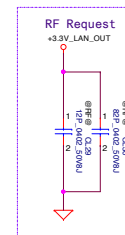
Compal Electronics, Inc.

eDP CONN & Touch screen

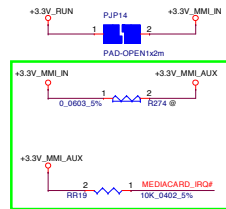
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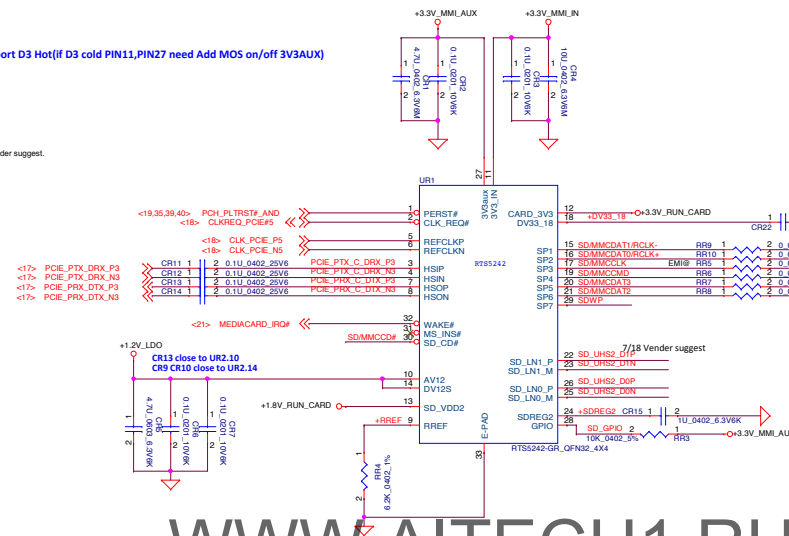
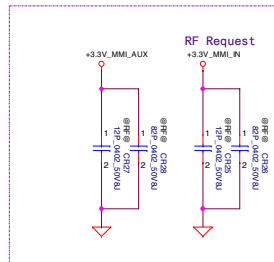


For PCIe Interface



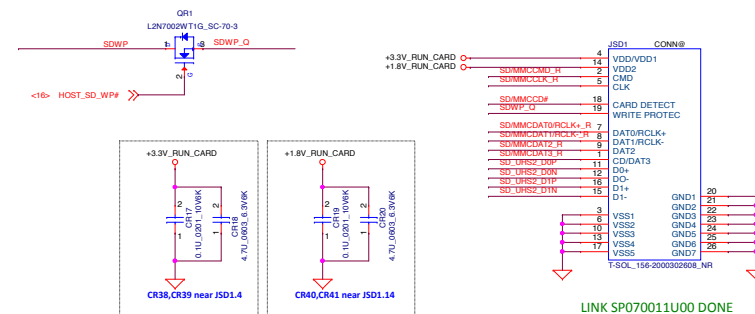
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.



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HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)



LINK SP070011U00 DONE

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Card Reader

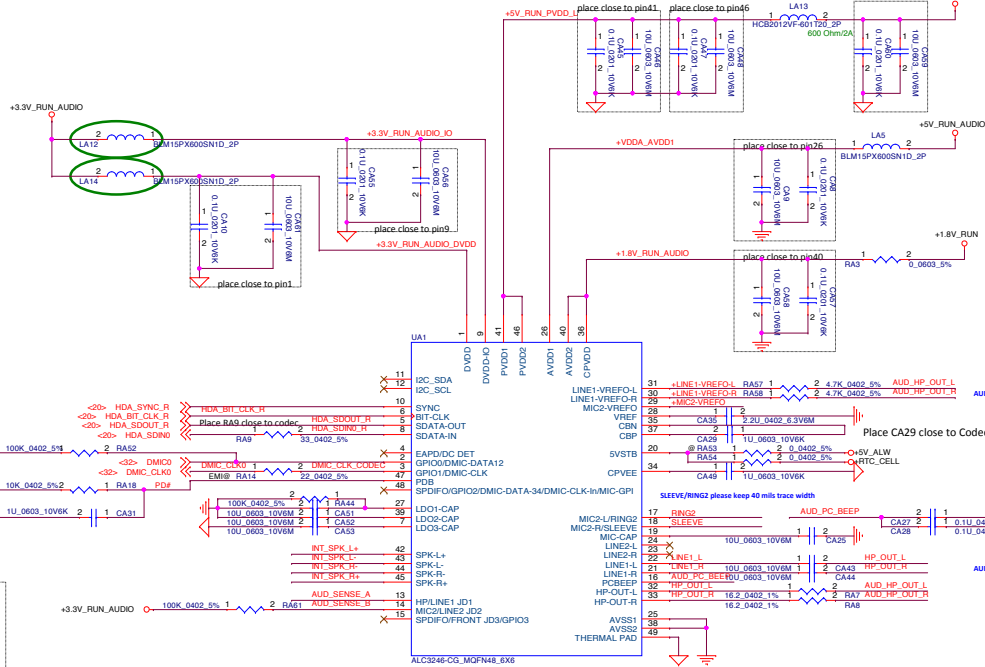
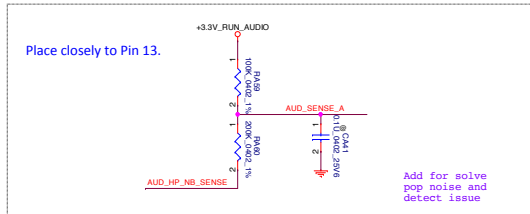
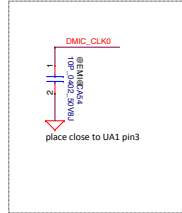
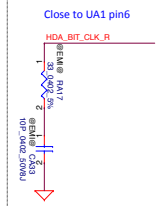
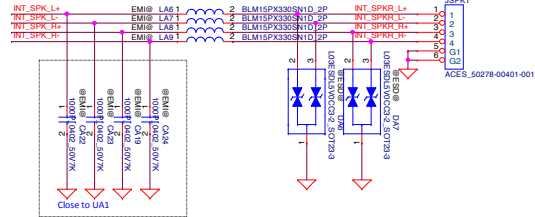
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		Sheet						61	

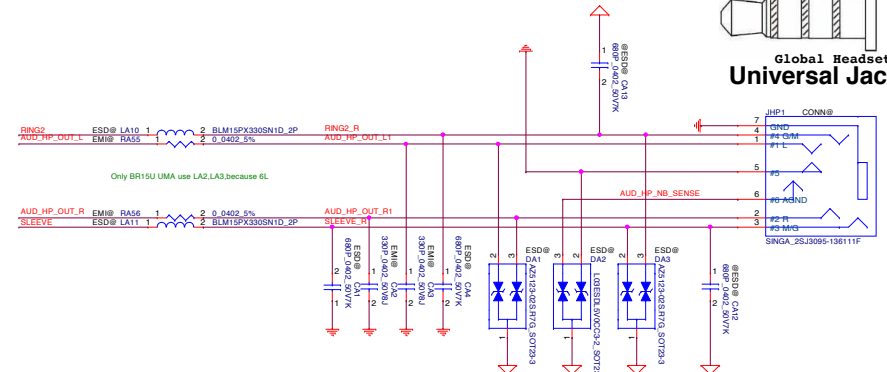
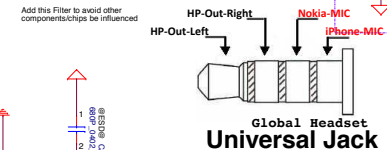
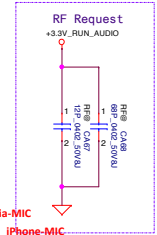
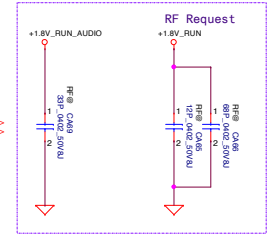
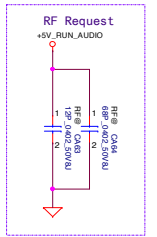
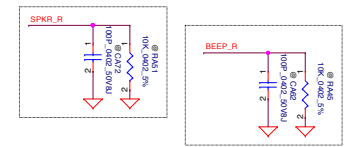
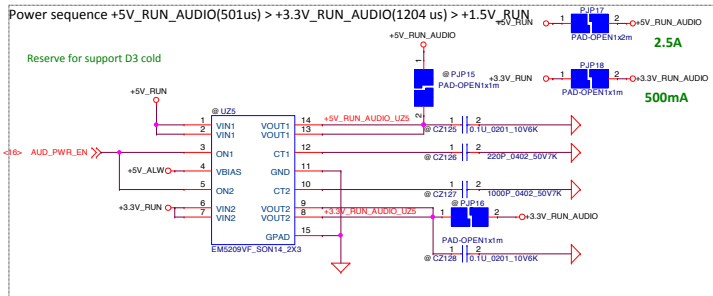
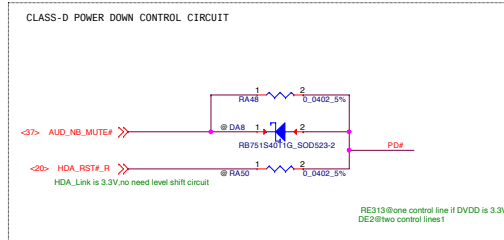
1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box)

Internal Speakers Header

40 mils trace keep 20 mil spacing

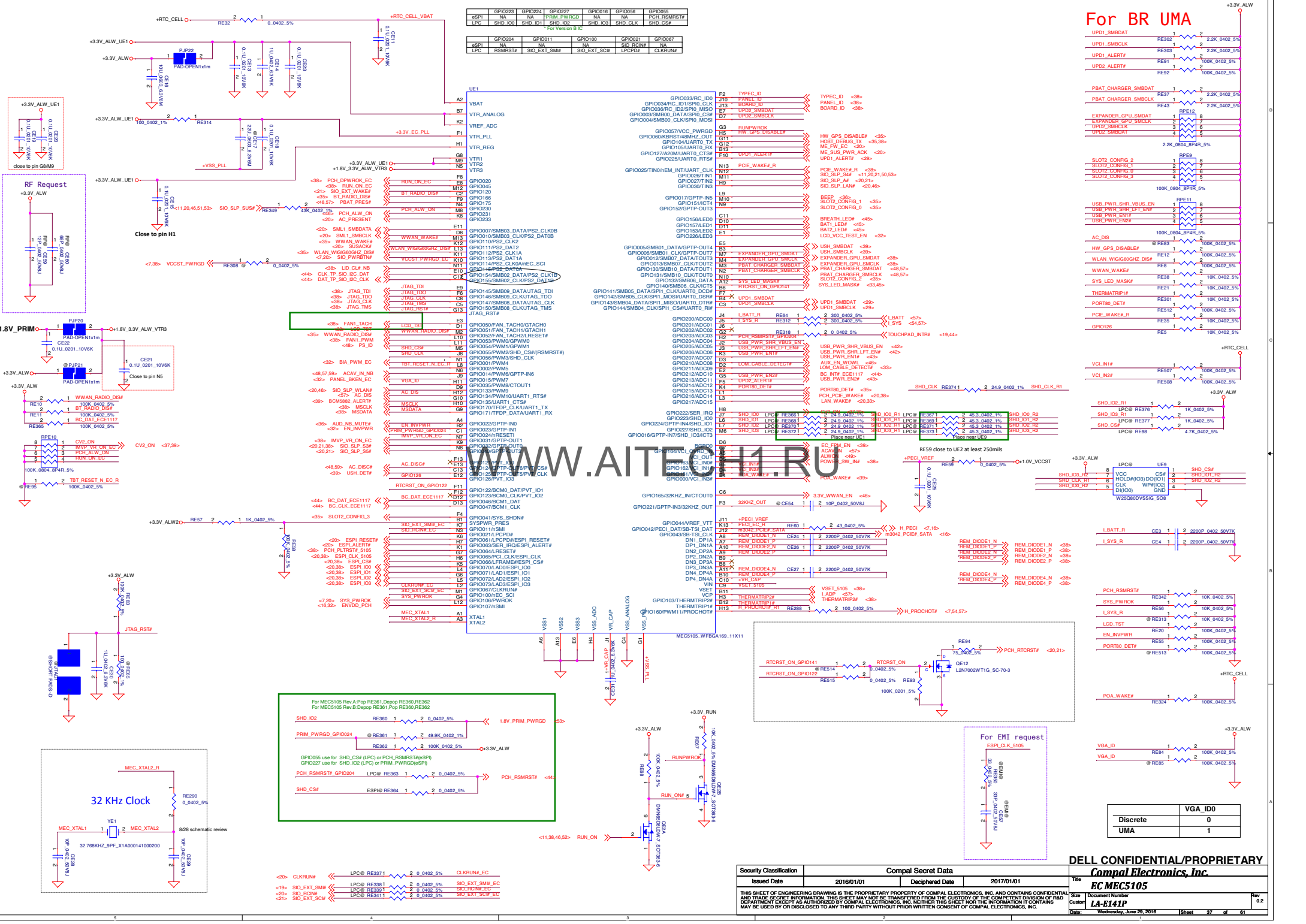


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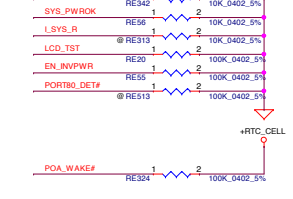
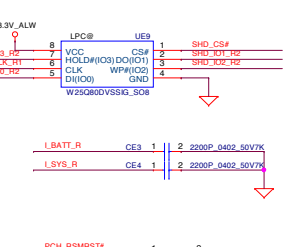
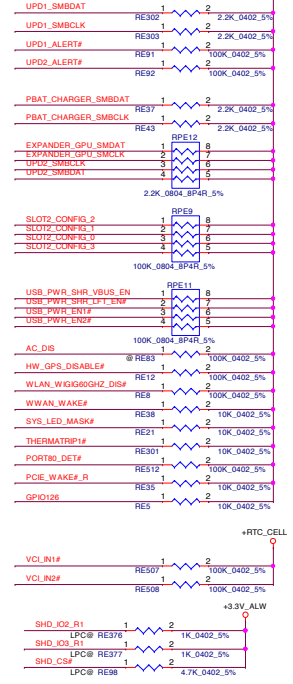


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Codec ALC3246



For BR UMA

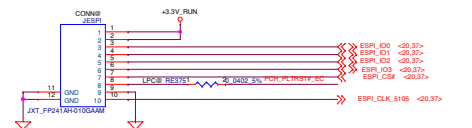
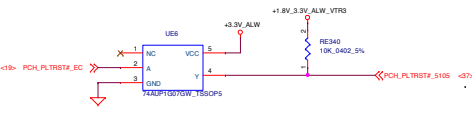


VGA_ID0	
Discrete	0
UMA	1

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EC MEC5105

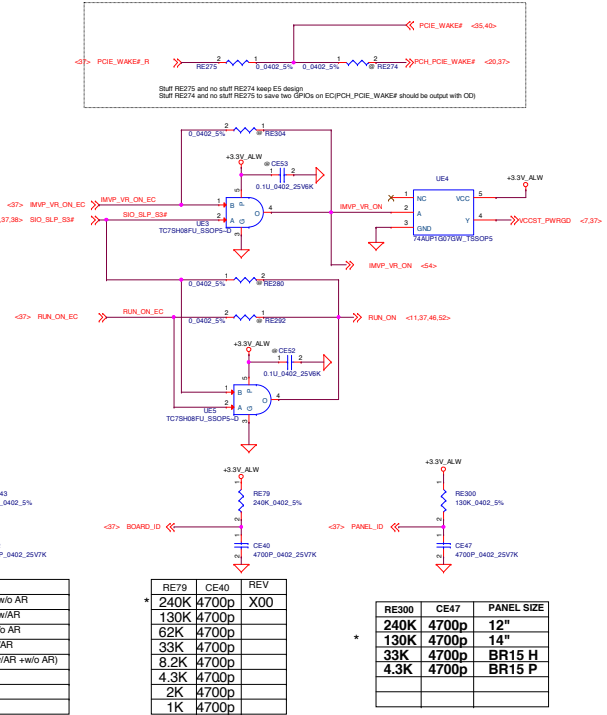
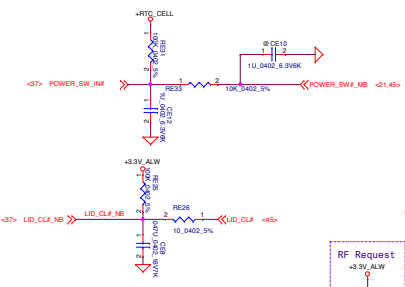
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LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	



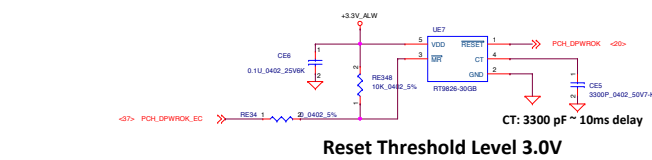
RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

RE79	CE40	REV
240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	BR15 H
4.3K	4700p	BR15 P

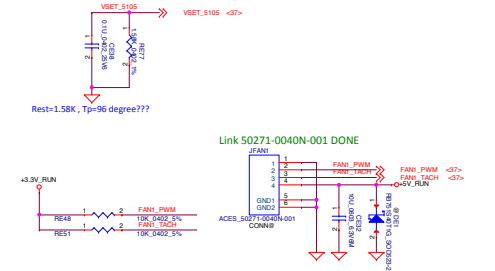
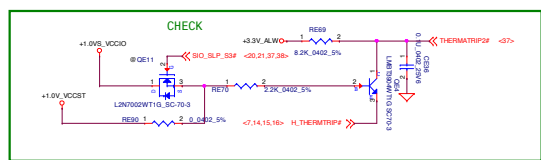
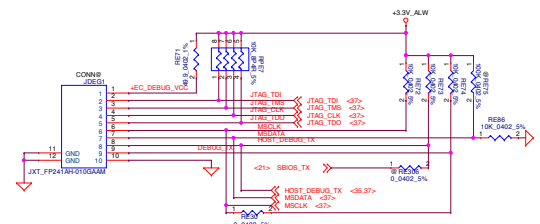
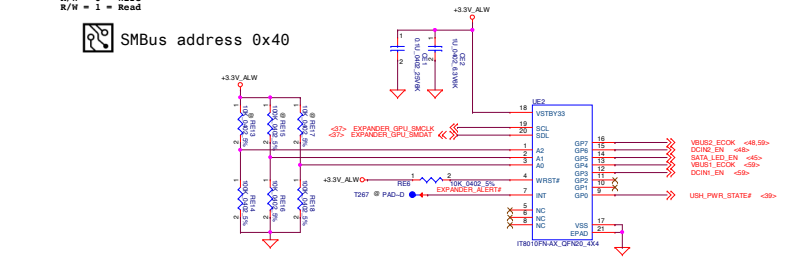
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PD_ACE_DET# rise time is measured from 5%~68% BOARD_ID rise time is measured from 5%~68% PANEL_ID rise time is measured from 5%~68%

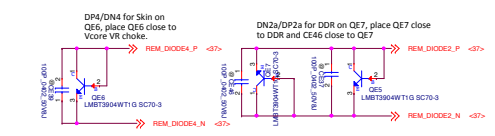


Control Byte
0 1 0 0 A2 A1 A0 R/W
R/W = 0 = Write
R/W = 1 = Read

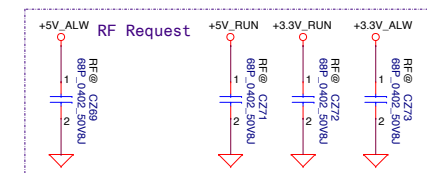
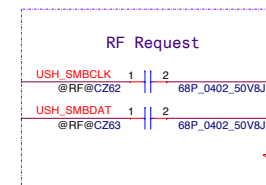
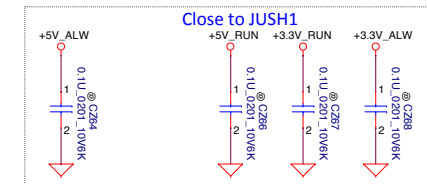
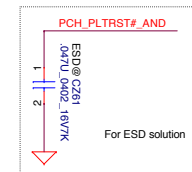
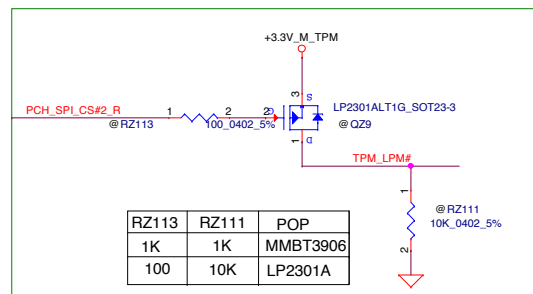
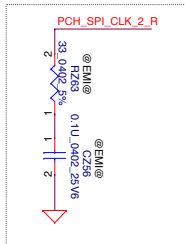
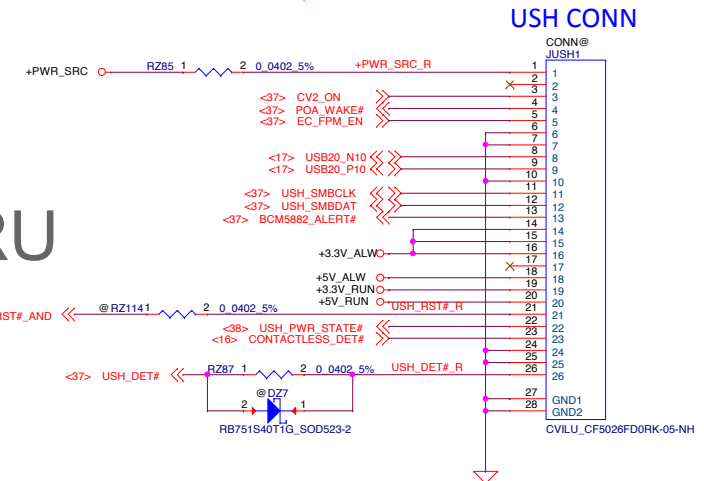
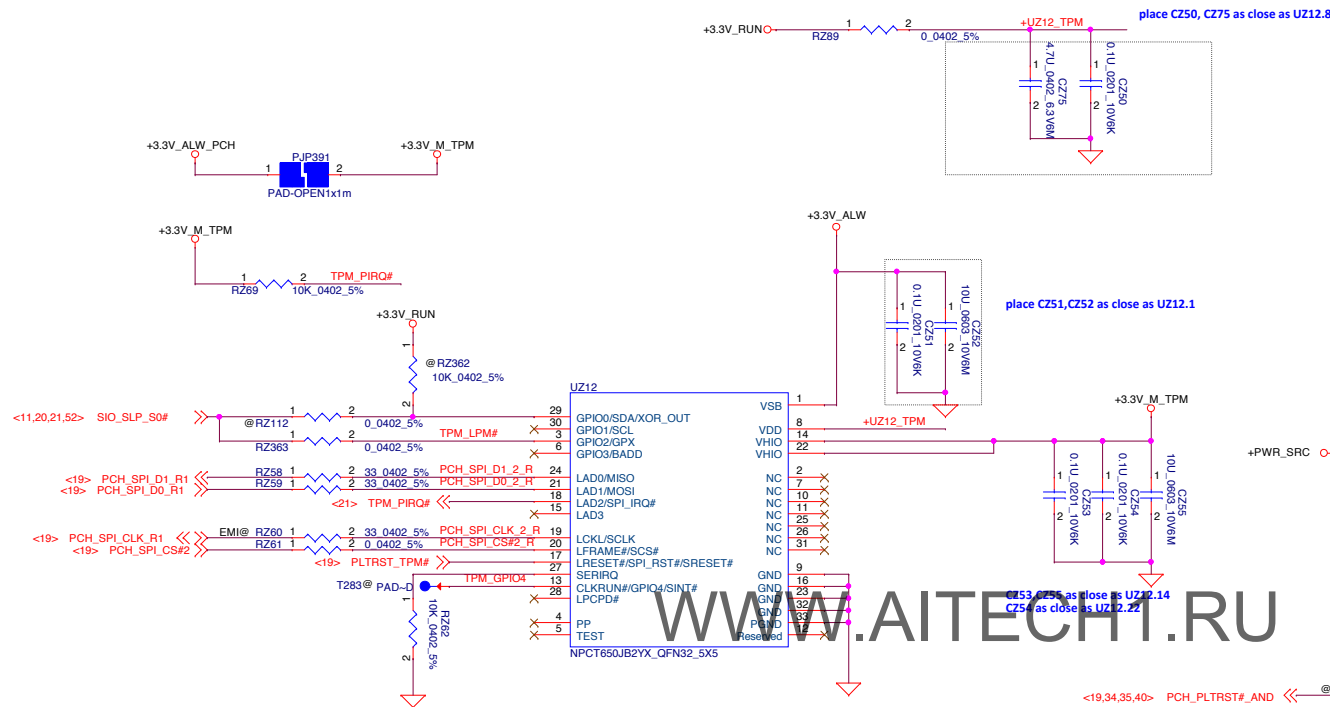
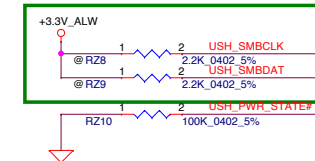
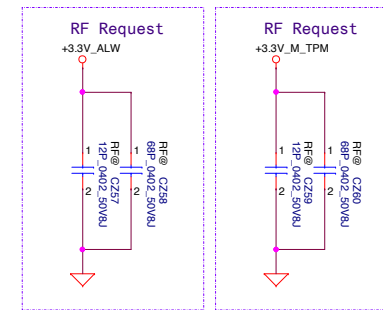
SMbus address 0x40



5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



For NUVOTON TPM



RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A

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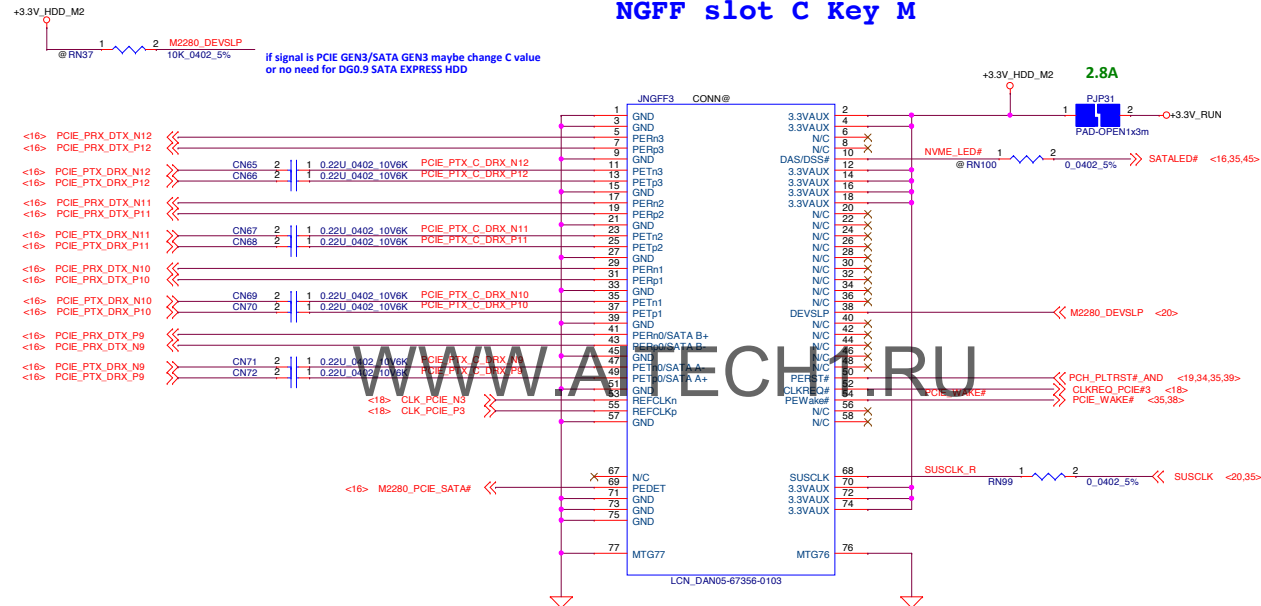
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

USH & TPM

IDENTIFICATION OF RECORDS SERIES	Document Number LA-E141P	Rev 0.2
Custom		
Date: Wednesday, June 29, 2016	Sheet 39 of 61	

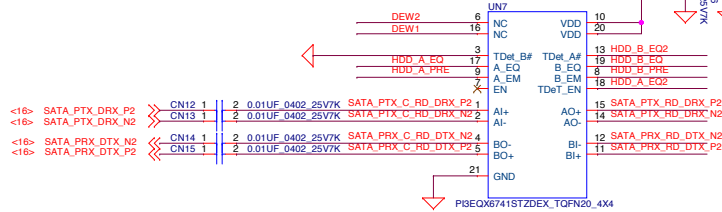
NGFF slot C Key M



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				B	Rev
				Date:	Wednesday, June 29, 2016

	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDeT_B#	NC	TDeT_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

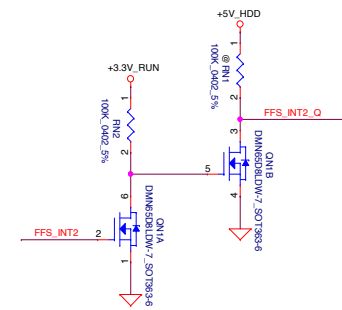
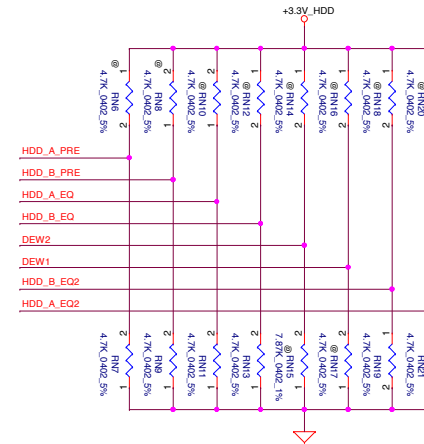
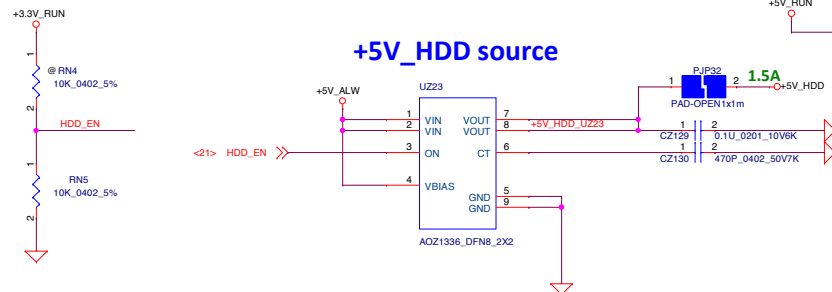
SATA Repeater



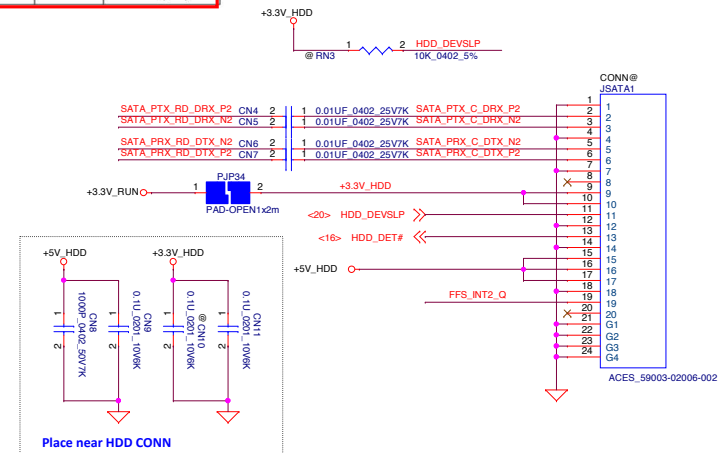
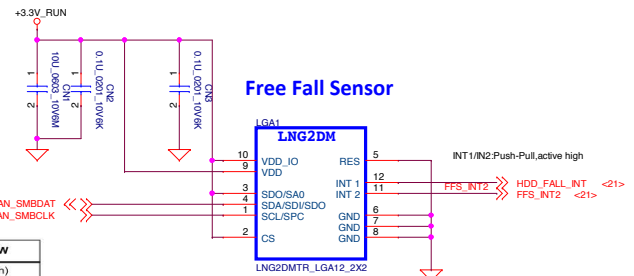
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	PD (RN5)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 NC 1	0dB -3.5dB -1.5dB	0dB -3.5dB -1.5dB

* red color is current setting

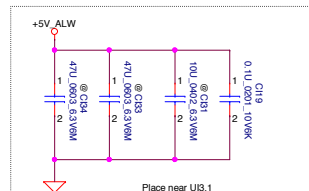
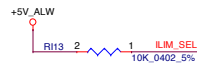
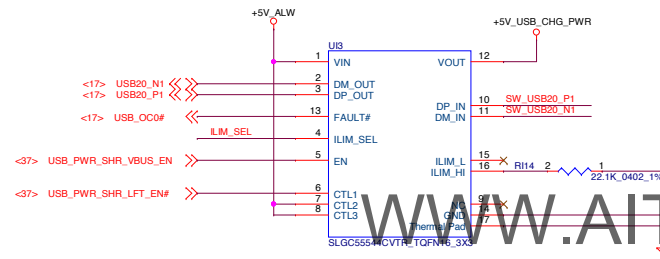
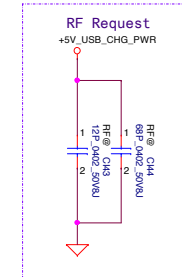
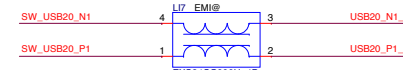
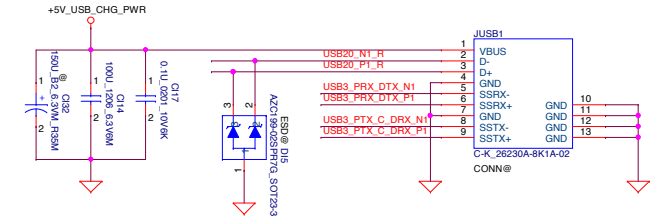
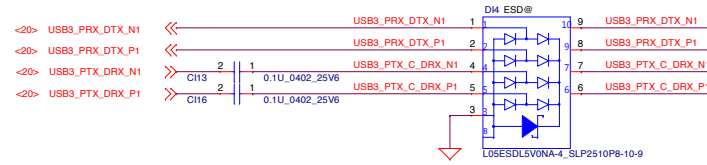


Free Fall Sensor



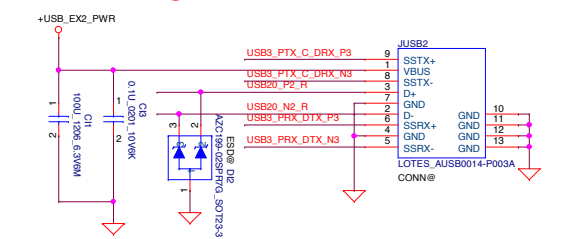
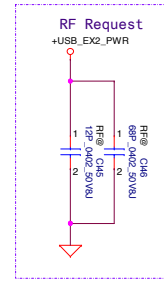
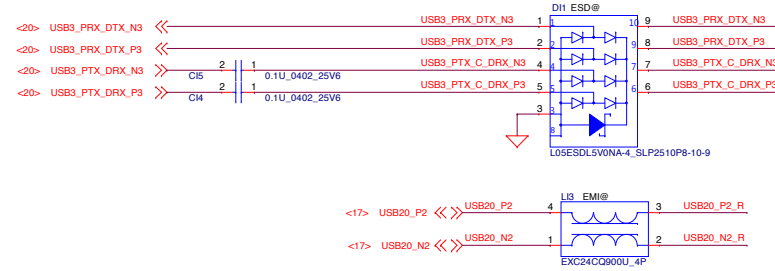
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Date: Wednesday, June 29, 2016		Sheet		41		of 61	

For PWR SW + Charger combine IC

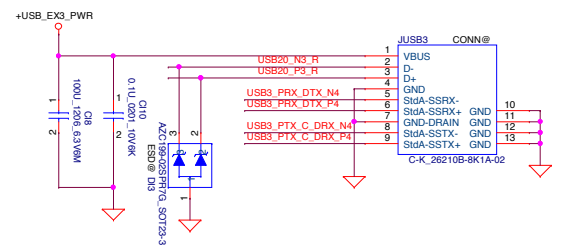
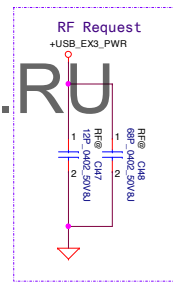
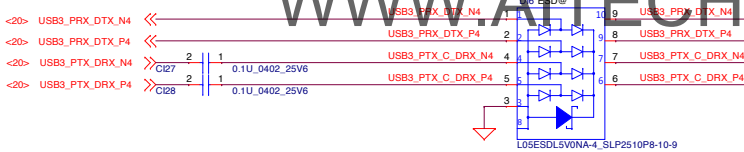
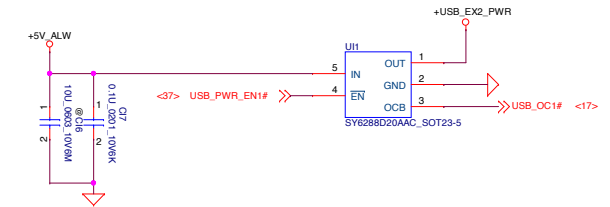


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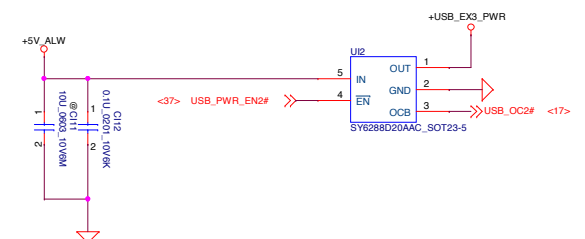
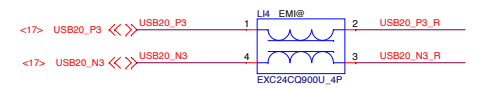
For Breckenridge 14&15/Steamboat 14



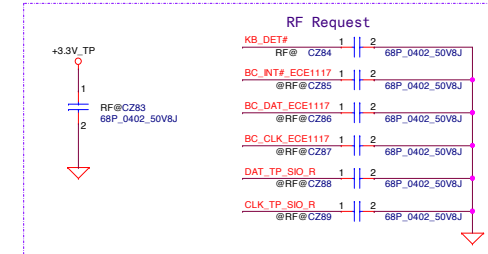
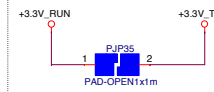
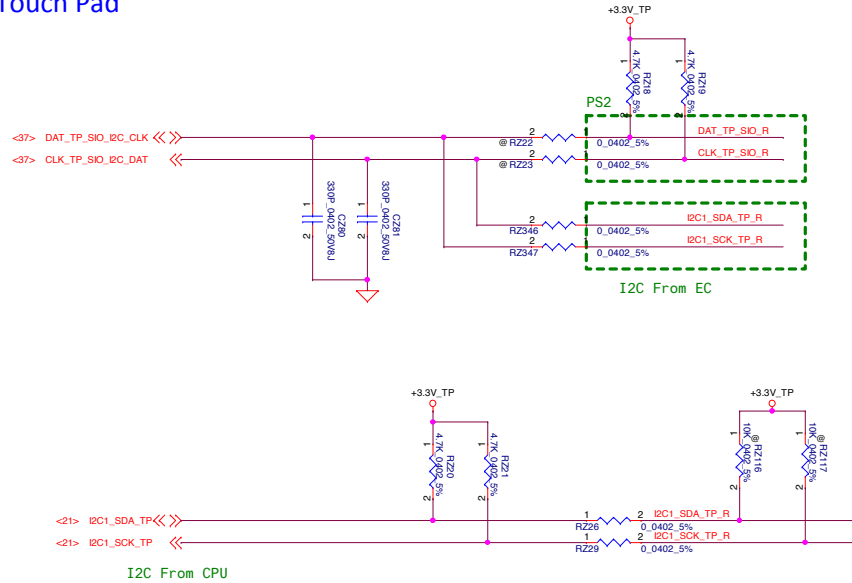
DfB request:
main SM070003200 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm



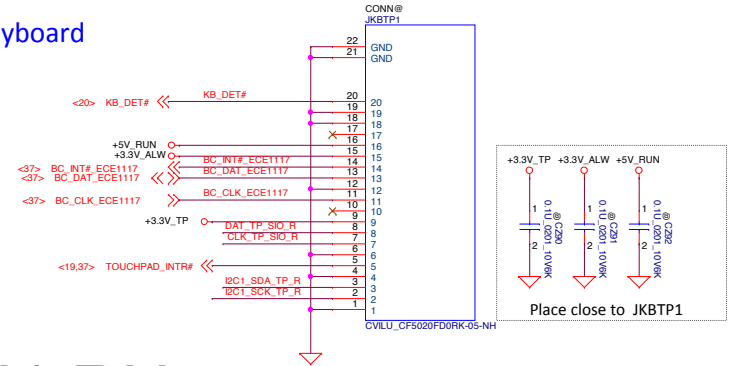
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Touch Pad

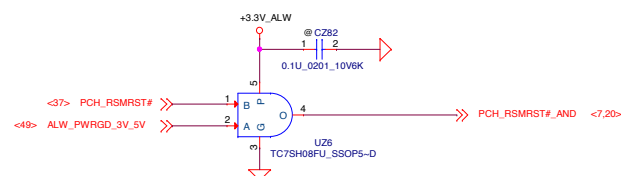


Keyboard



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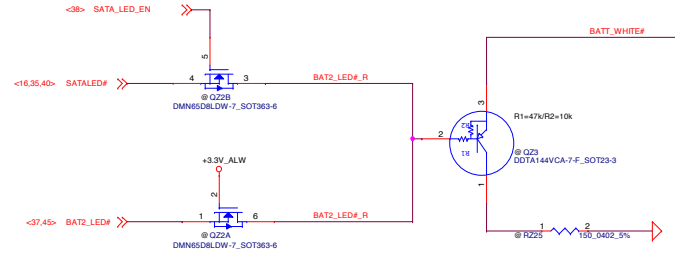
RSMRST circuit



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							Document Number
							LA-E141P
							Rev
							0.2
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							44 of 61

HDD LED MUX

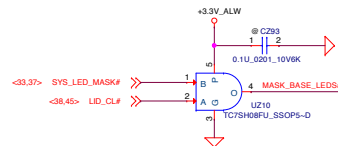
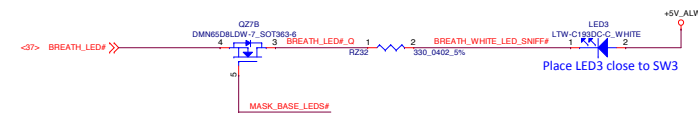
means EC can switch battery white led and HDD LED by hot key "Fn+H"



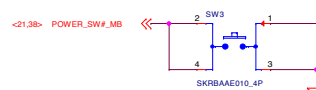
Battery LED



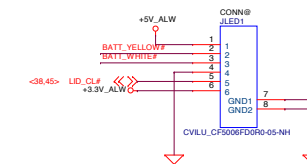
Breath LED



POWER & INSTANT ON SWITCH



LED board CONN

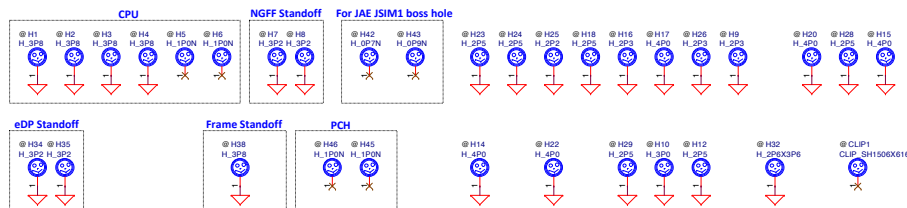


Fiducial Mark



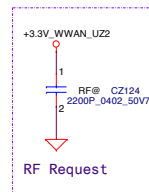
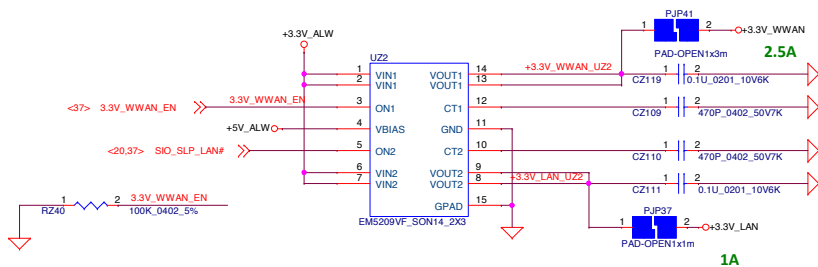
LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

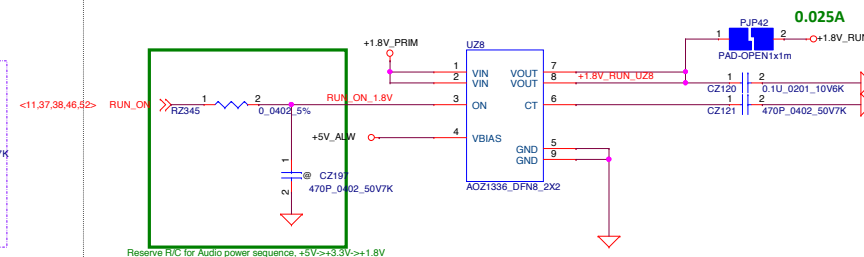


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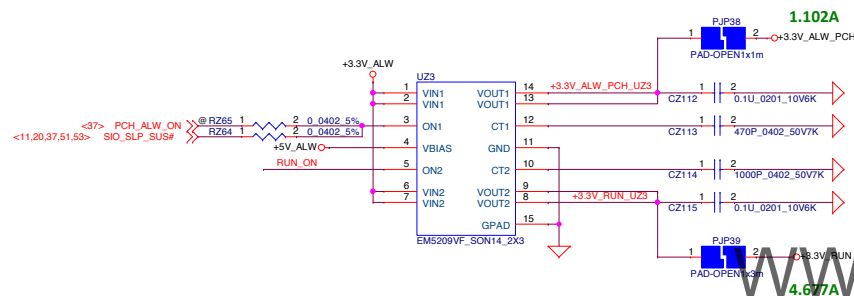
+3.3V_WWAN/+3.3V_LAN source



+1.8V_RUN source

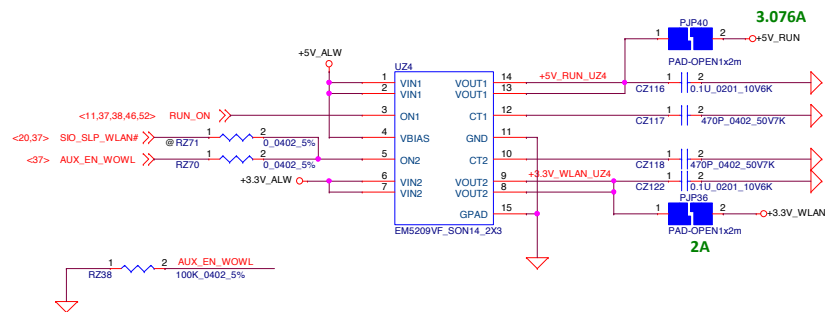


+3.3V_ALW_PCH/+3.3V_RUN source



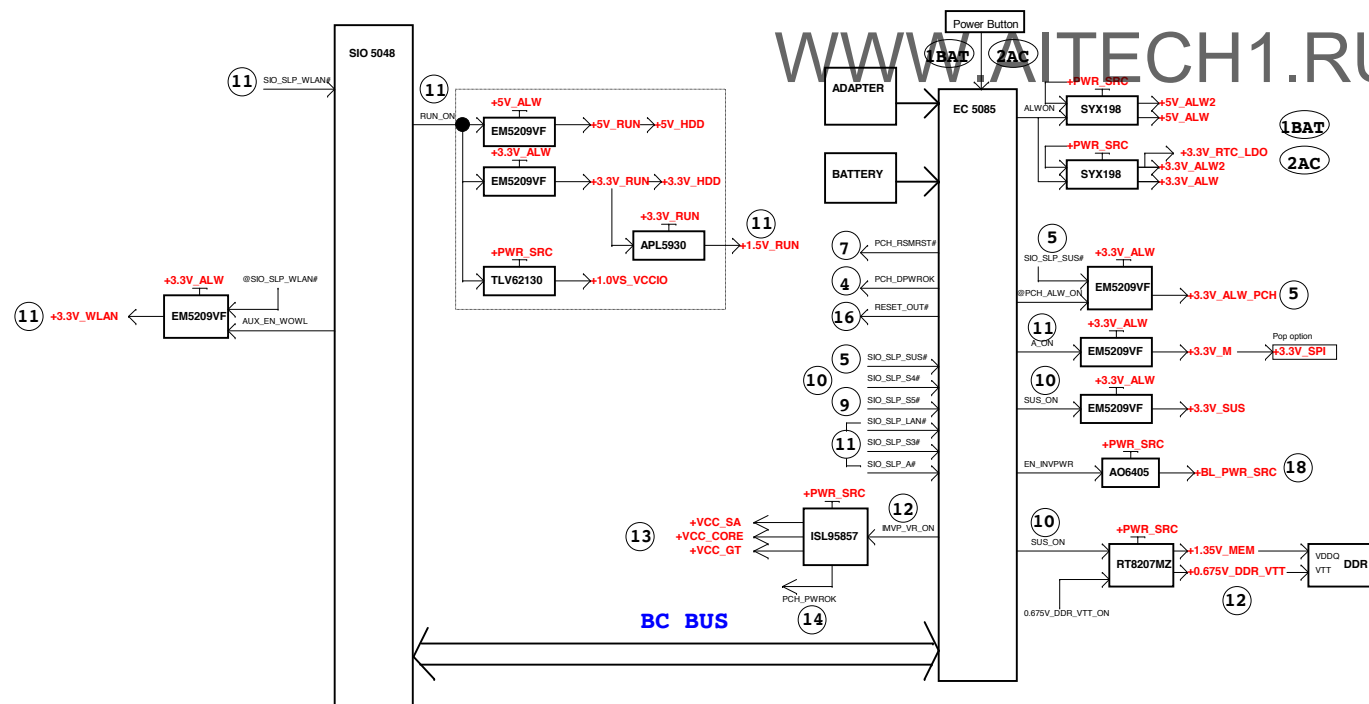
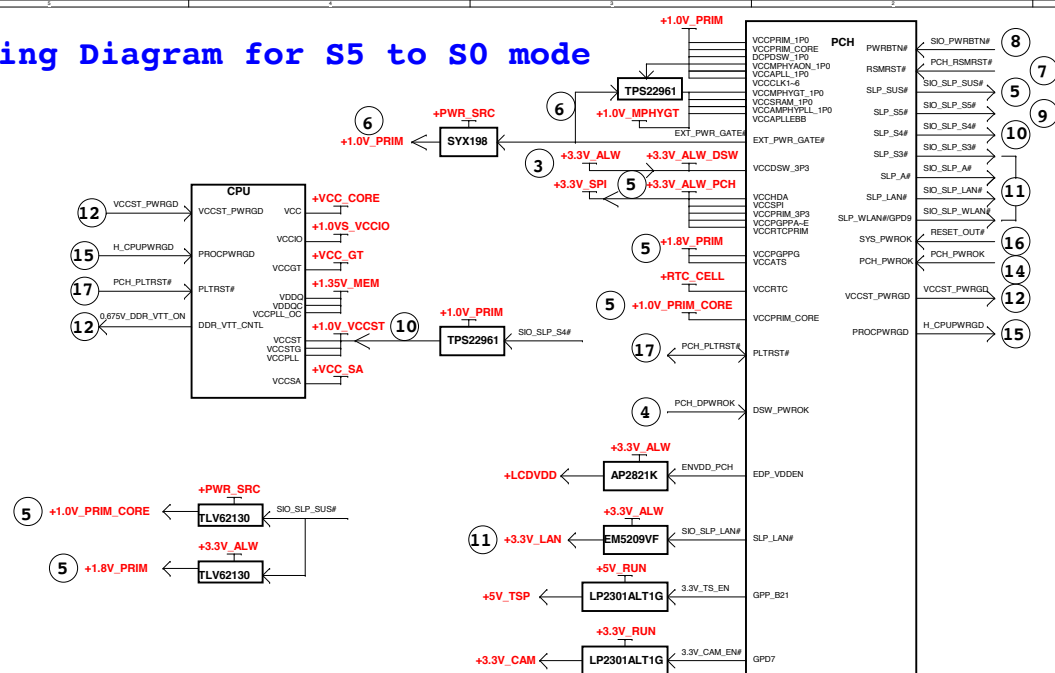
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+5V_RUN/+3.3V_WLAN source



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Timing Diagram for S5 to S0 mode



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			Revision 1 of 1	Page 1 of 1

+PWR_SRC

PJP100
PAD-OPEN 1x2m-D

+3.3V_ALW

PGOOD_3V

3V5V_EN

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+PWR_SRC

PJP101
PAD-OPEN 1x2m-D

+3.3V_ALW

PGOOD_5V

3V5V_EN

3V5V_EN

3V5V_EN

3V5V_EN

3V5V_EN

3V5V_EN

3V5V_EN

3V5V_EN

3V5V_EN

3V5V_EN

3V5V_EN

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+3.3V_ALWP

JUMP_43X118

+5V_ALWP

JUMP_43X118

+5V_ALWP

JUMP_43X118

+5V_ALWP

JUMP_43X118

+5V_ALWP

JUMP_43X118

+5V_ALWP

JUMP_43X118

+5V_ALWP

JUMP_43X118

+5V_ALWP

JUMP_43X118

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Compal Electronics, Inc.

+5V_ALW/3.3V_ALW

Document Number

LA-E141P

Date

Wednesday, June 29, 2016

Rev

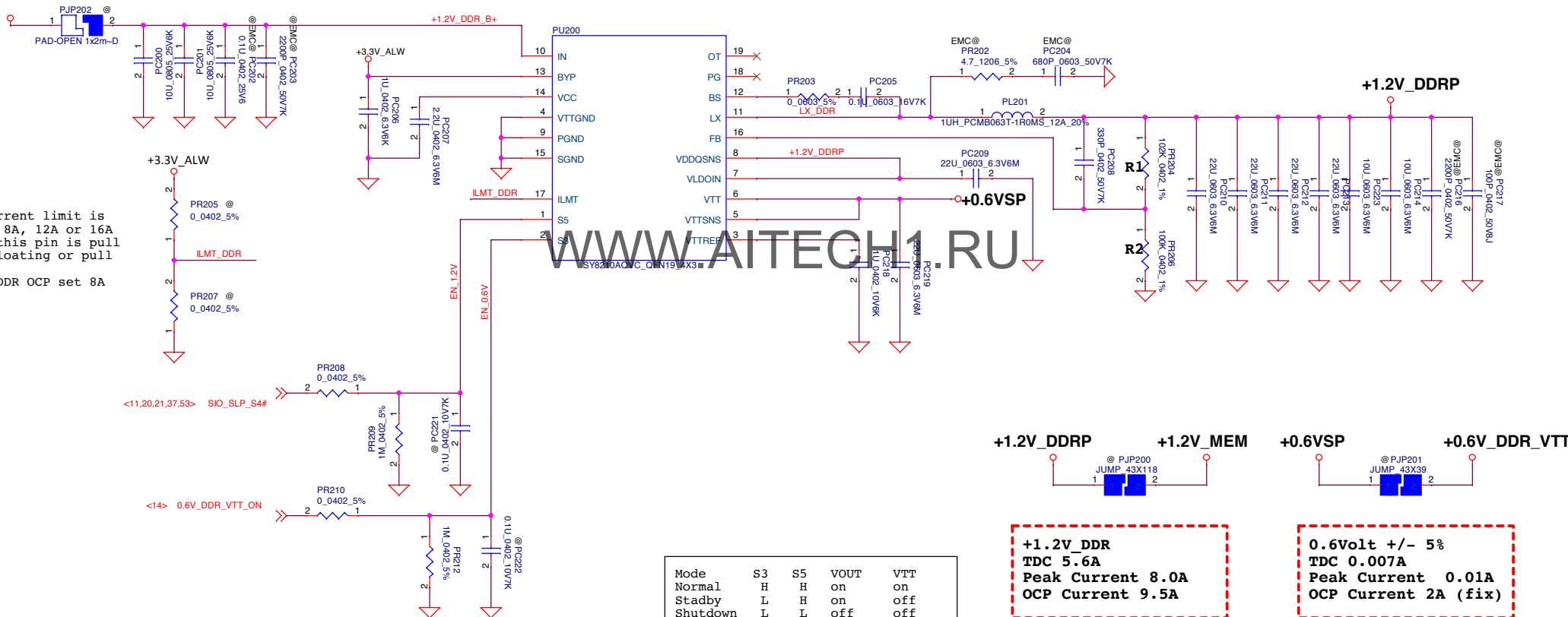
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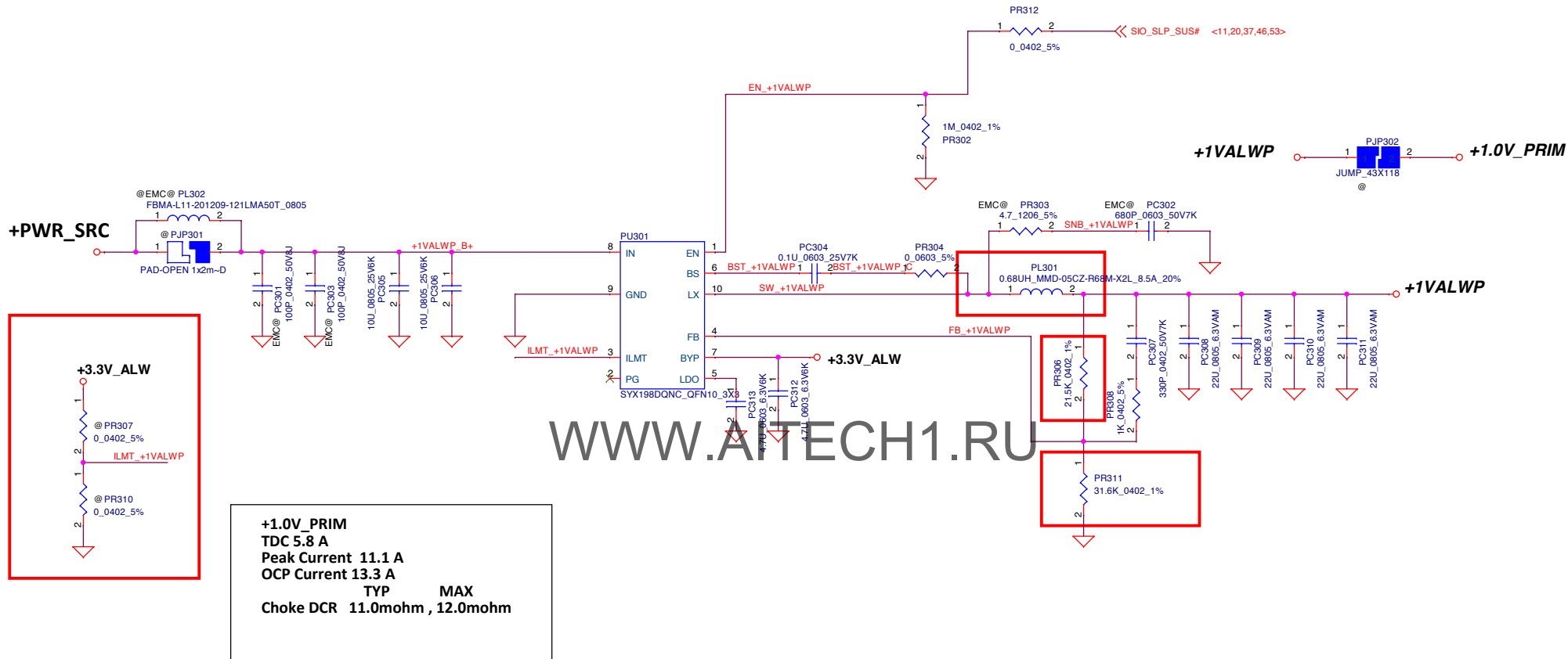
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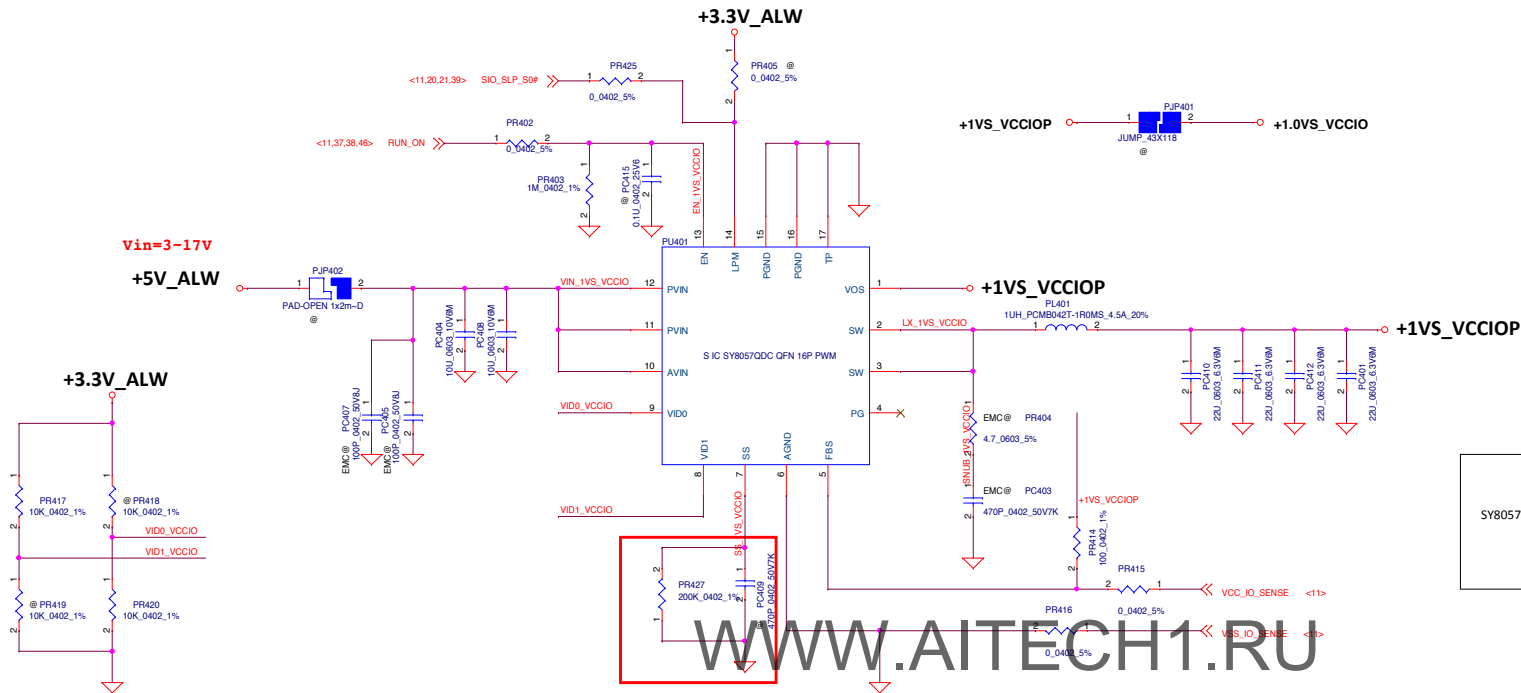
+PWR_SRC





The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

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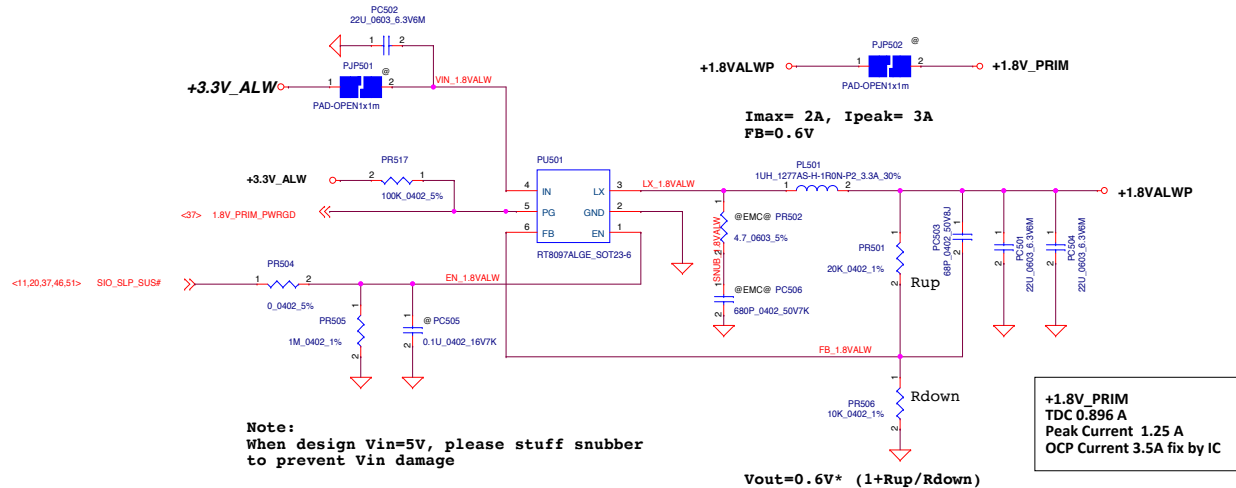


+1.0VS_VCCIO
TDC 3.9A
Peak Current 5.5 A
OCP Current 6.6 A Fix by IC
TYP MAX

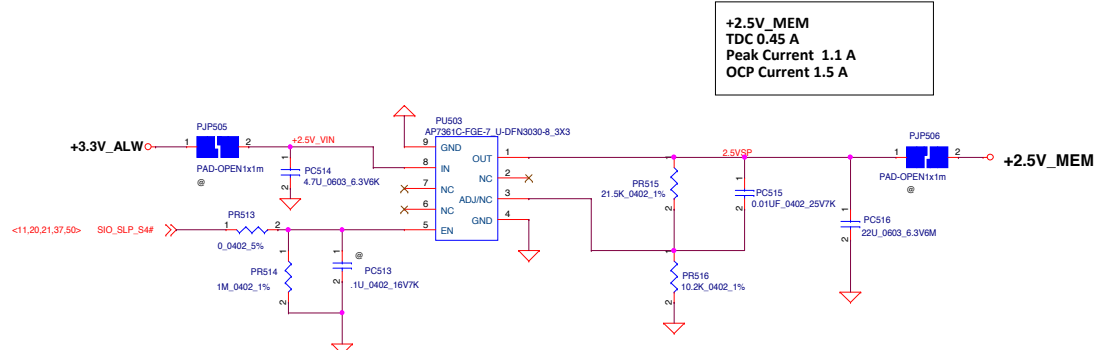
	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
SY8057	0	X	X	0(LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

Preset the different pull down resistor to choose the required power rail

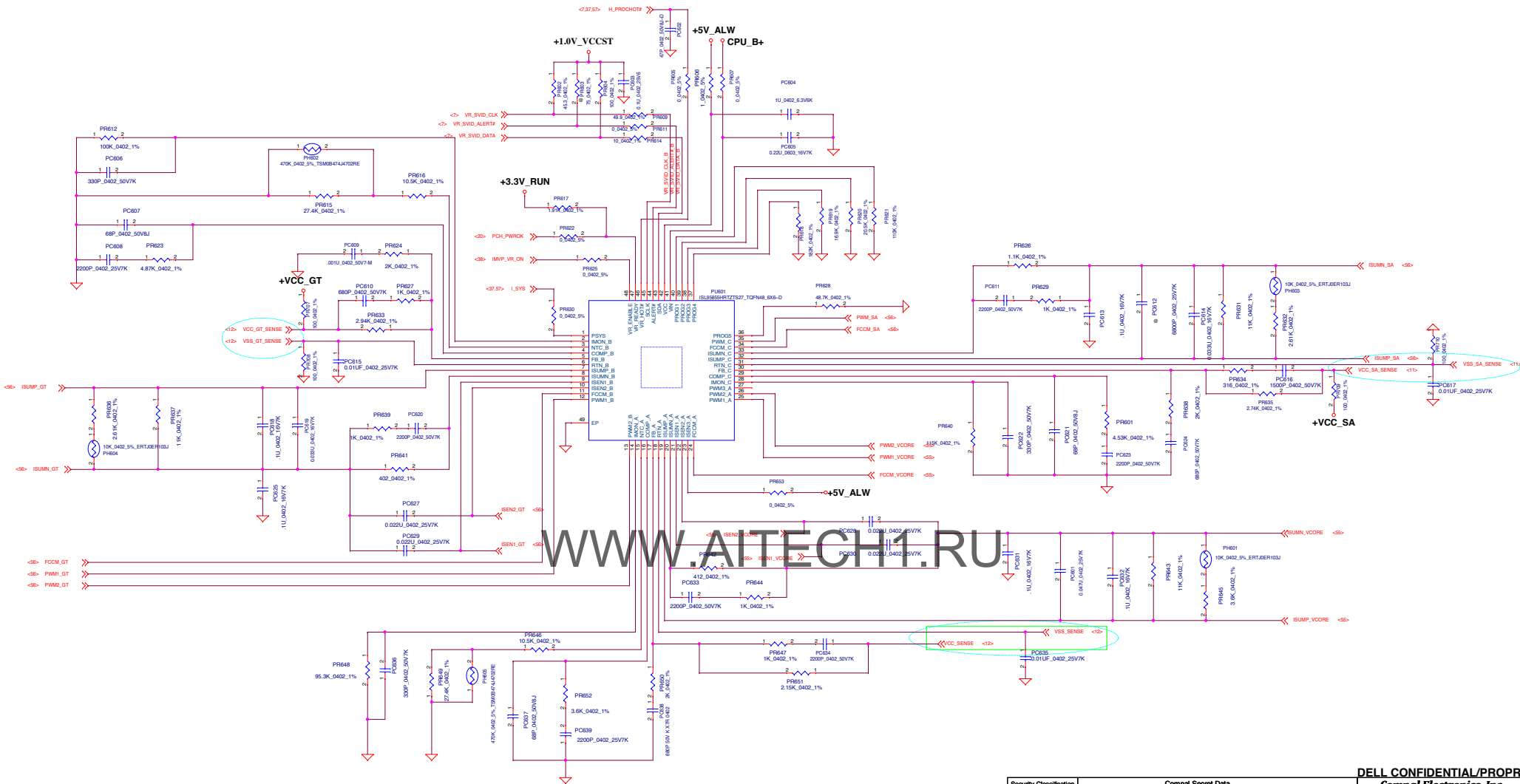
(VCCIO/PCH/EDRAM/EOPIO applications.)
RMODE>500k or floating Vcc_PRIM_CORE.
RMODE=200k Vcc_IO.
RMODE=0 Vcc_EDRAM.



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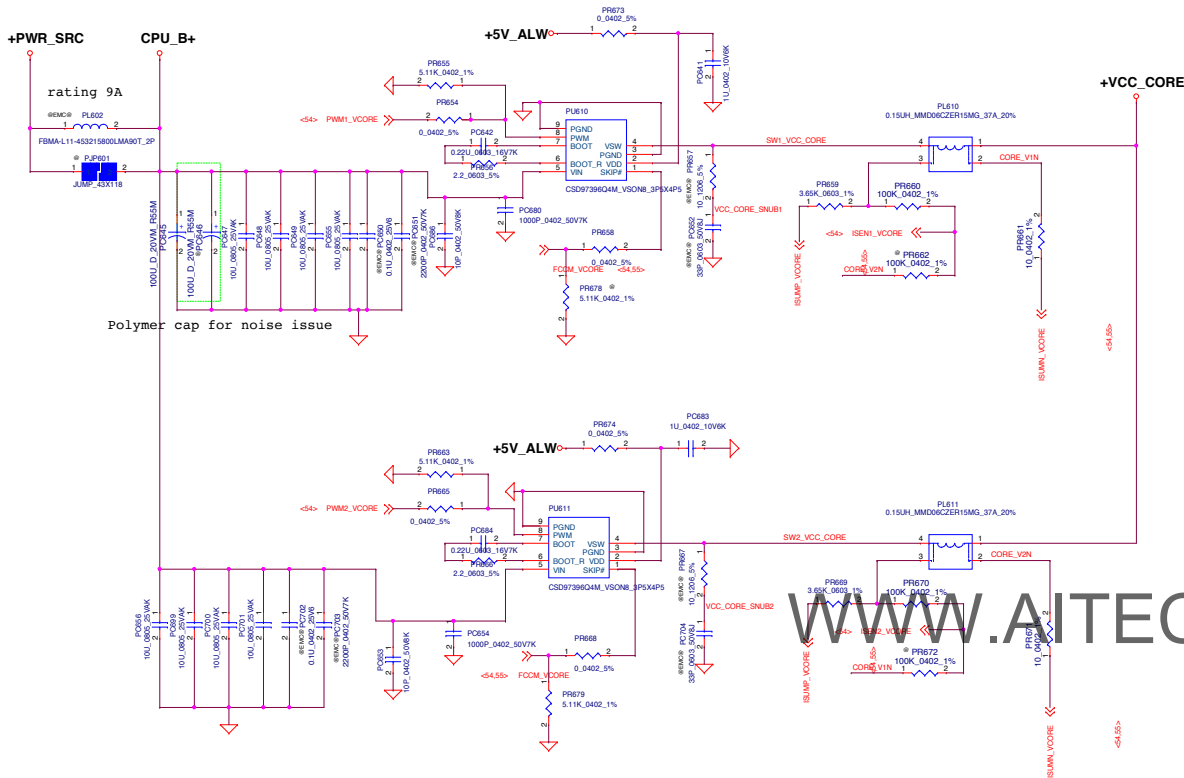
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Title		DELL CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc. +1.8VALWP/+1.5VSP/2.5V_MEM	
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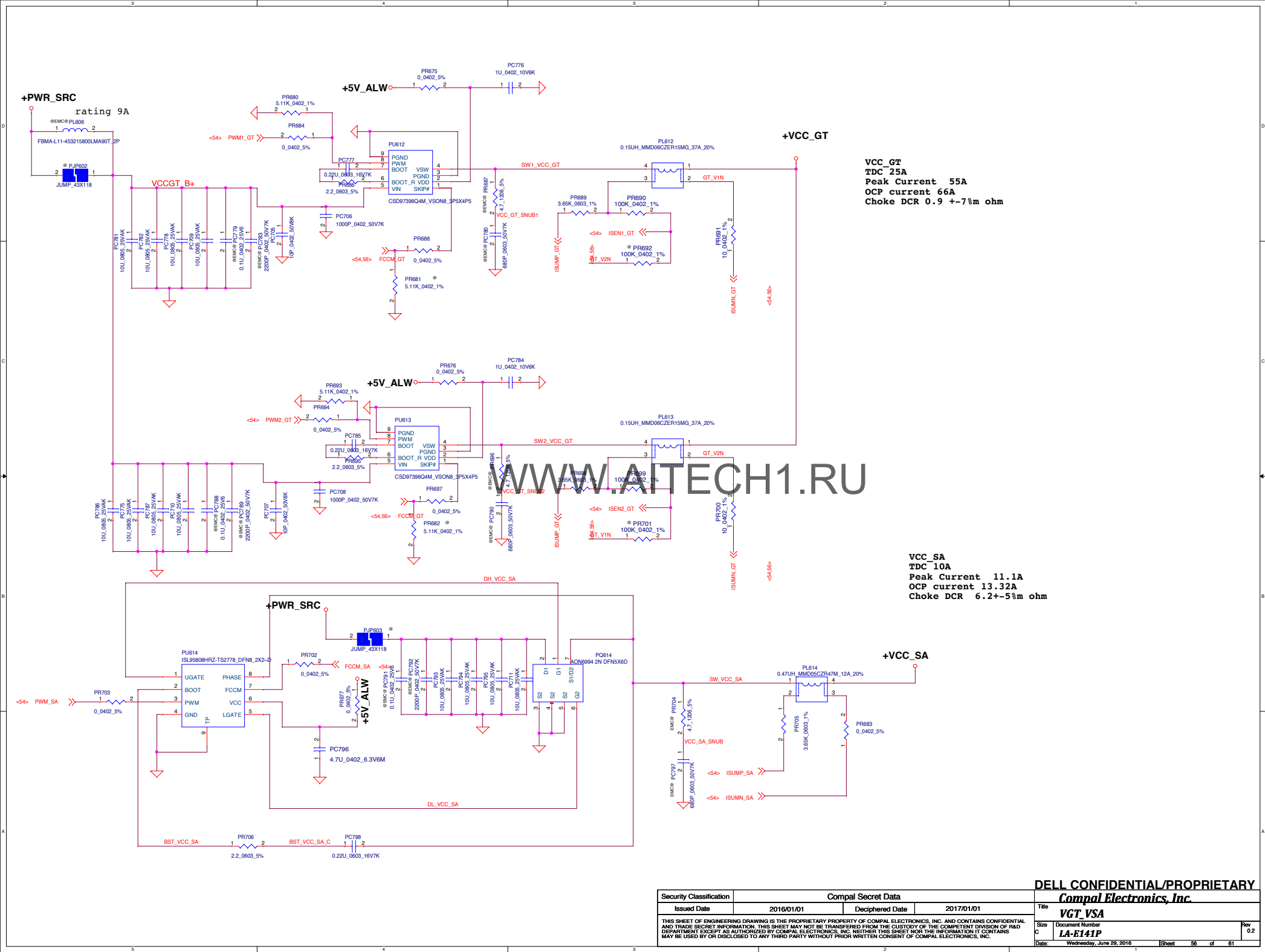
VCC_core
TDC 50A
Peak Current 60A
OCP current 81.6A
Choke DCR 0.9 +-7% ohm

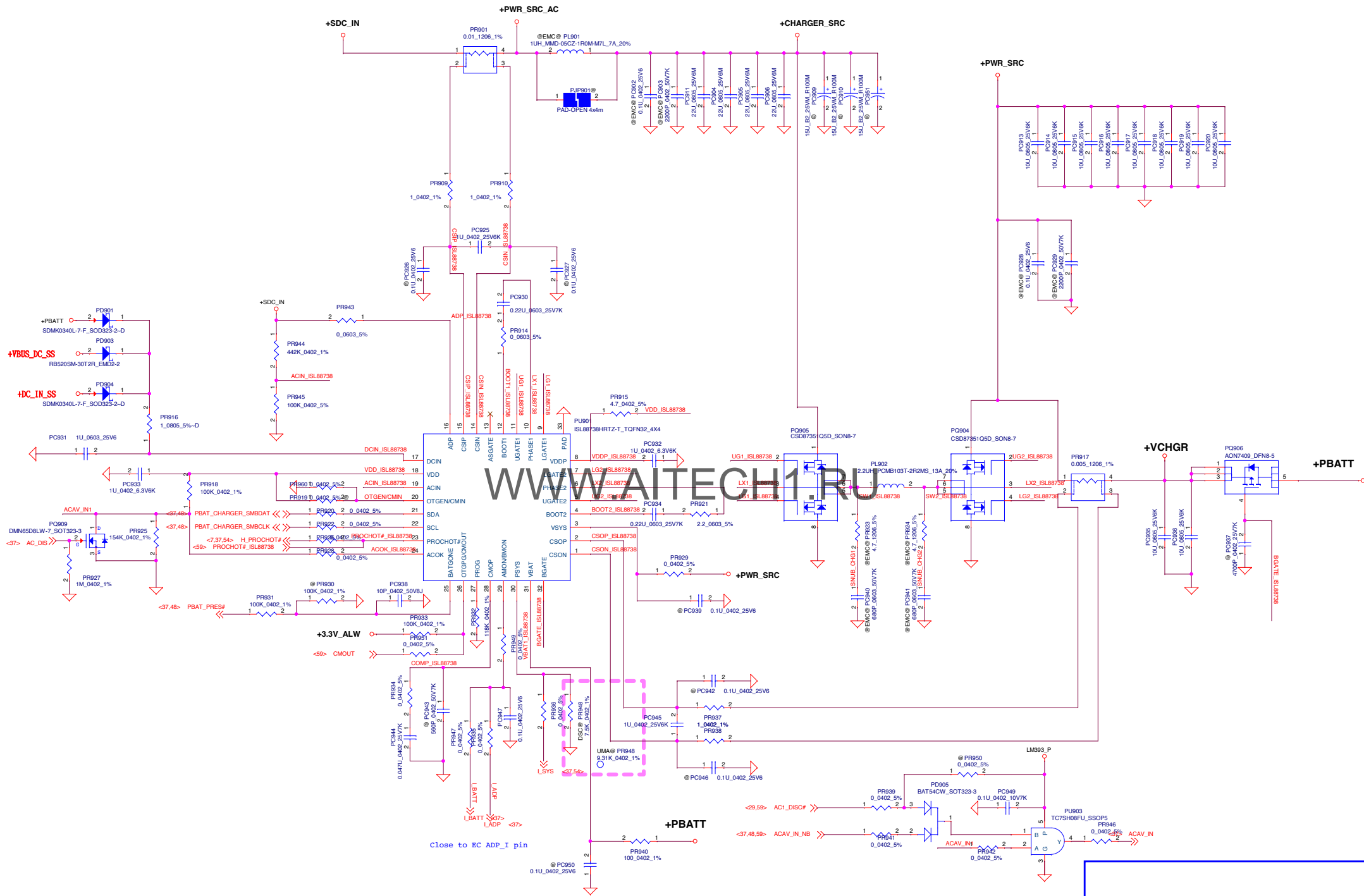


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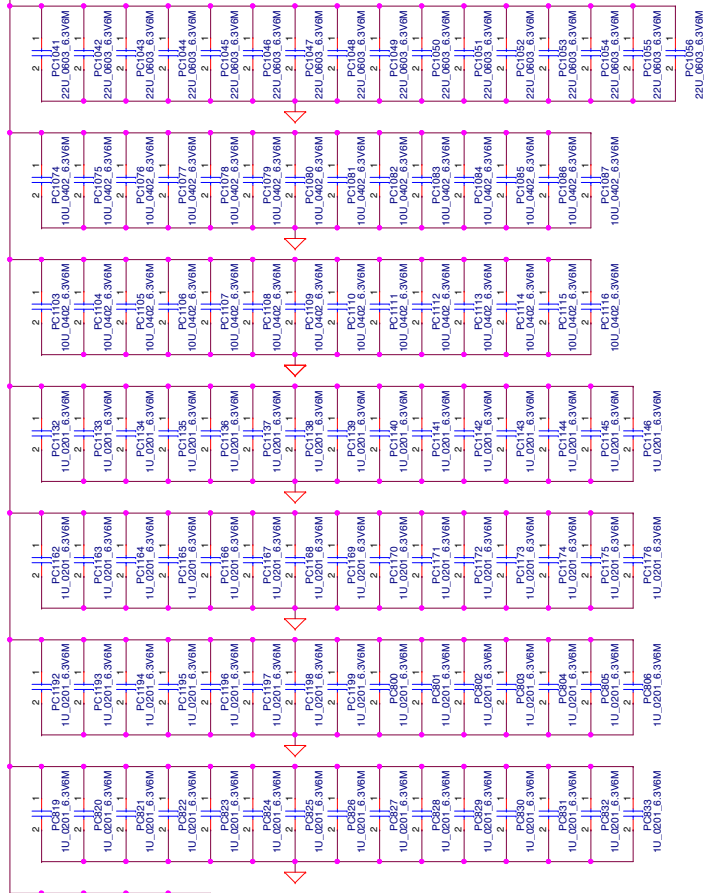
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Issued Date	2016/01/01	Deciphered Date	2017/01/01
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Title		VCCORE	
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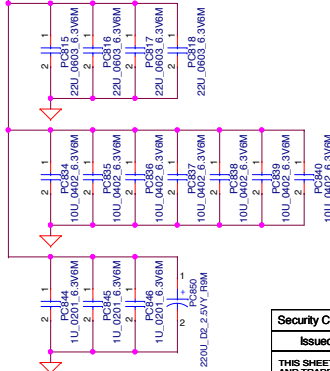


+VCC_CORE

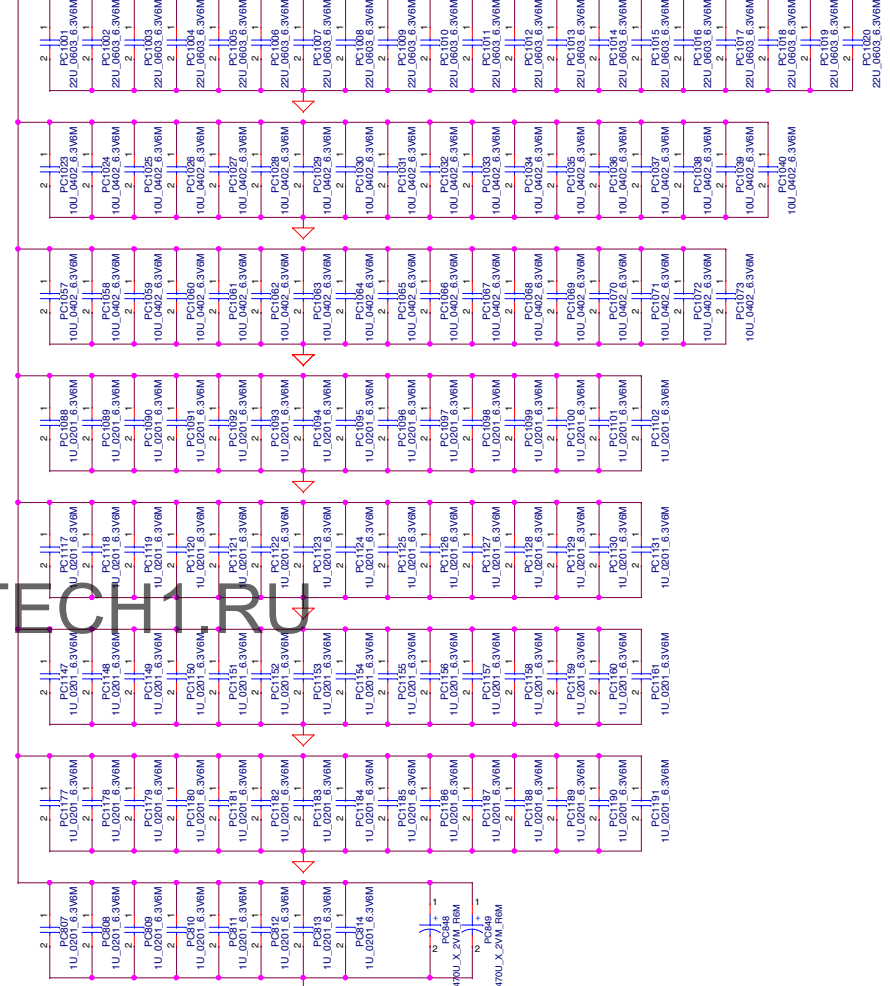


VCC_SA Place on CPU
Back Side.
22U_0603 * 2 pcs + 10U_0402*7 pcs + 1U_0201*3 pcs
Primary Side.
22U_0603 * 2 pcs + 220u_D2*1 pcs

+VCC_SA



+VCC_GT



VCC_GT Place on CPU
Back Side.
22U_0603 * 8 pcs + 10U_0402*35 pcs + 1U_0201*68 pcs
Primary Side.
22U_0603 * 12 pcs + 470u_D2*2 pcs

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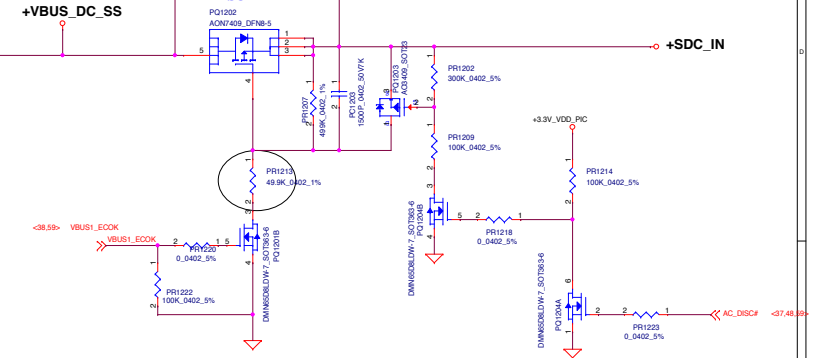
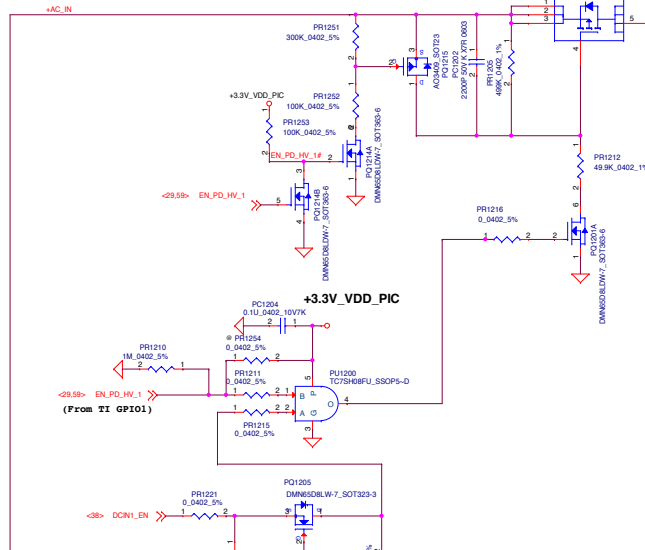
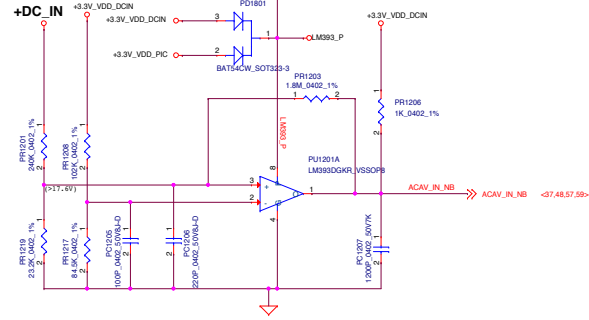
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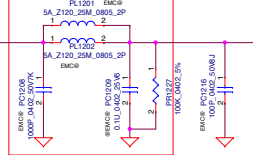
DCIN_AC_Detector



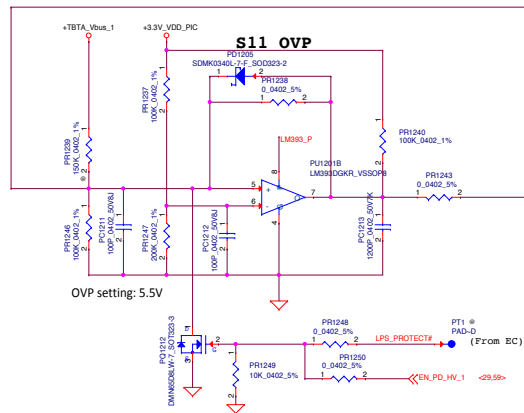
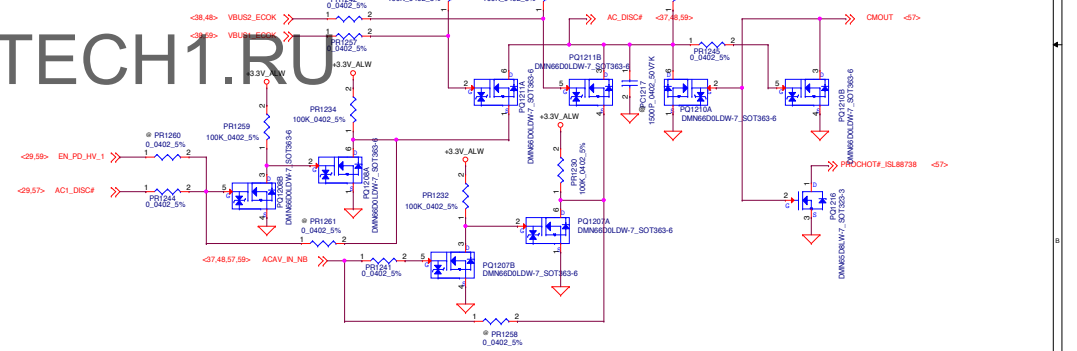
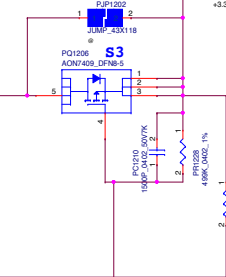
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+TBTA_VBUS

EMI Part



PC1209 can't over 1000P



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				SELL OR CONFIDENTIAL/PROPRIETARY	
Investment				General Electronic No.	
Account	Symbol	Quantity	Price	POWERS	
				14000	

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	HW	2016/5/27	COMPAL	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
2	37	HW	2016/5/27	COMPAL	Reserve PORT80_DET# PD resistance	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
3	35	HW	2016/6/1	COMPAL	Intel schematics reivew modify item	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(0)_0201 to 10uF_0603	0.2(X01)
4	39	HW	2016/6/1	COMPAL	TPM change to NUVOTON	Change TPM from Atmel to NUVOTON.	0.2(X01)
5	35	HW	2016/6/1	COMPAL	Intel reviw result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
6	35	HW	2016/6/7	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
7	37	HW	2016/6/7	COMPAL	For MEC5105K-D1-TN setting	1. Change UE1 to SA00009GL00 2. POP RE360,RE362 3. De-POP RE361	0.2(X01)
8	35,32	HW	2016/6/16	COMPAL	For EMC request	De-pop RZ131, RZ132. CL22 change to 10pf , POP CA7,CZ1 (100P),CH268 modify from 22p to 47p and POP,Change LV1 to SM01000NY00	0.2(X01)
9	41	HW	2016/6/16	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	POP RN5	0.2(X01)
10	39	ME	2016/6/17	COMPAL	Connector change	1. JKBTP1 change to CVILU_CF5020FDORK-05-NH 2. JUSH1 change to CVILU_CF5026FDORK-05-NH 3. JIR1 change to ACES_50208-0060N-P01	0.2(X01)
11	36	HW	2016/6/20	COMPAL	Vender suggest	RA7,RA8 change to 16.2ohm	0.2(X01)
12	37	HW	2016/6/22	COMPAL	The posibility of GPIO map update	Add RE514,RE515 for RTCRST_ON	0.2(X01)
13	41	HW	2016/6/22	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)

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